MT8385 IoT Application Processor Datasheet

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Version History

Version	Date	Description
1.0	2021-10-01	First official release
1.1	2023-01-11	• Modified Table 5-2 Storage Conditions • Modified max. value of operating junction temperature in Table 5-3 Recommended Operating Conditions
1.2	2023-04-12	• Modified Section 3.12.1.2 I2C Timing Characteristics • Modified AVDD12_SSUSB to AVDD18_SSUSB in Table 4-5 Pin Characteristics
1.3	2023-06-01	• Modified Bluetooth 5.0 to Bluetooth 4.2 in Table 1-1 Device Features
1.4	2024-03-29	• Modified the part number in Table 1-2 Ordering Information

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1 Introduction

The MT8385 is a highly integrated and powerful IoT platform with the following key features:

- Quad-core Arm® Cortex®-A73 processor
- Quad-core Arm Cortex-A53 processor
- Arm Mali™-G72 MP3 3D Graphics Accelerator (GPU) with Vulkan® 1.0, OpenGL ES 3.2 and OpenCL™ 2.x full profile
- Dual-core Vision Processor Unit (VPU) Cadence® Tensilica® VP6 DSP
- LPDDR3 or LPDDR4/X external memory support
- HEVC/H.264 1080p @ 30fps video decoding
- H.264 1080p @ 30fps video encoding
- High-resolution, multi-camera framework, up to 32MP @ 30fps
- Display support with MIPI® DSI, and DPI/DBI outputs, up to 2400p × 1080p (Full HD+), 20:9 aspect ratio
- eMMC5.1 and UFS2.1 interfaces
- Advanced Wi-Fi®, Bluetooth®, GNSS, and FM Radio connectivity

Figure 1-1 shows the functional block diagram of the device.

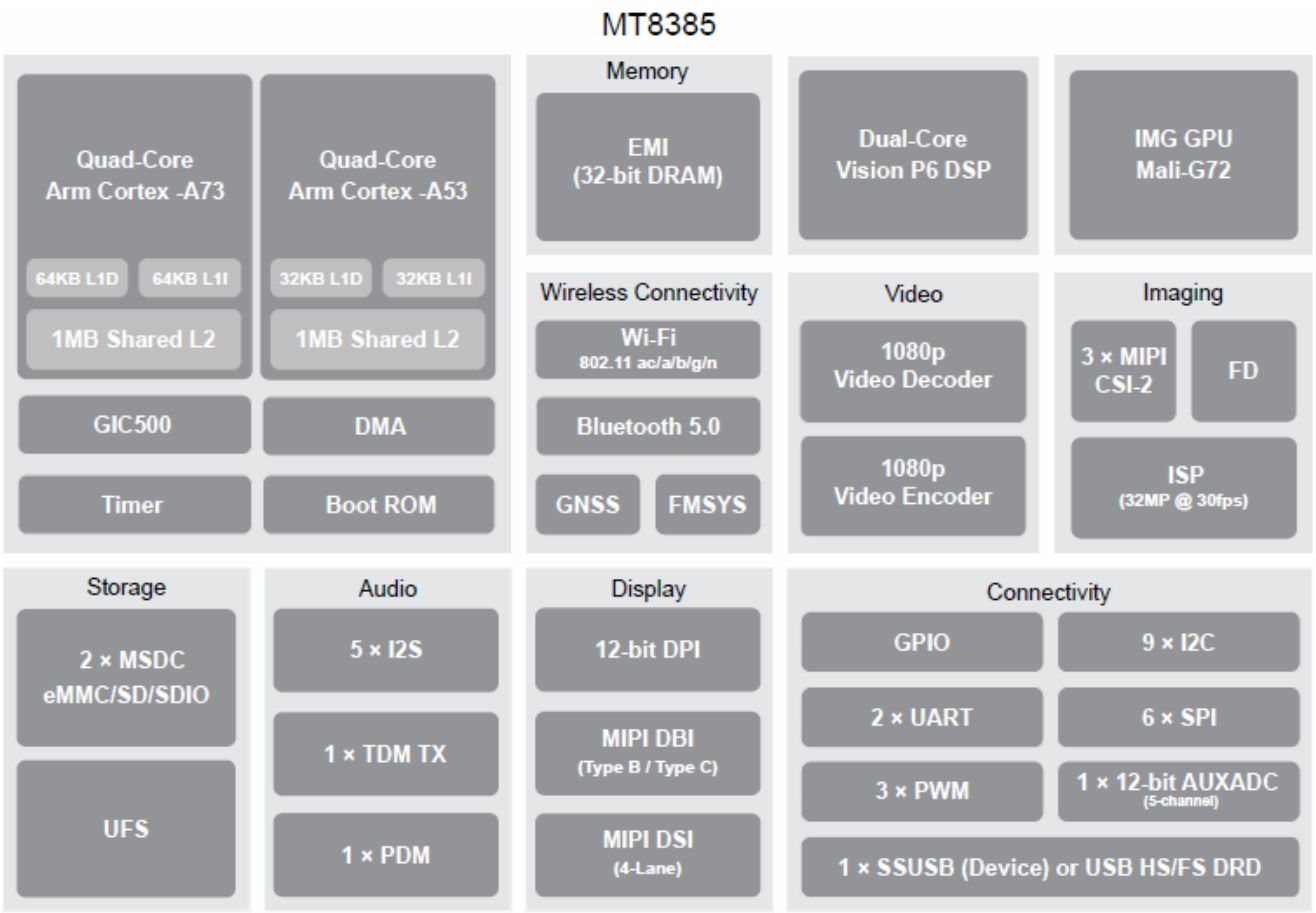


Figure 1-1 Functional Block Diagram

1.1 Features Overview

Table 1-1 shows a summary of the device feature.

Table 1-1 Device Features

Feature		MT8385
Processors		
Quad-core Arm Cortex-A73	A73	Up to 2000 MHz (see Section 6.1)
Quad-core Arm Cortex-A53	A53	Up to 2000 MHz (see Section 6.1)
Graphics Accelerator Mali G-72 MP3	GPU	Up to 800 MHz (see Section 6.1)
Vision Processing Unit VP6 DSP	VPU	Up to 525 MHz (see Section 6.1)
Memory		
External Memory Interface (LPDDR3 and LPDDR4/X)	EMI	Up to 8GB DDR-3733 (see Section 6.1)
Storage		
Memory Card Controller eMMC™/SD®/SDIO	MSDC0	eMMC (8-bit)
	MSDC1	Wi-Fi / SD card (4-bit)
Universal Flash Storage	UFS	Yes (one-lane)
Display		
Display Controller	DISP	Concurrent dual display
Display Parallel Interface	DPI	12-bit(1)
MIPI Display Bus Interface	DBI	Type B (8-/9-bit) or Type C (Option 1/3) (1)
MIPI Display Serial Interface	DSI	4-lane
Imaging		
Image Signal Processor	ISP	32MP @ 30fps
MIPI Camera Serial Interface 2	CSI	3 × 4-lane D-PHY or 2 × 4-lane D-PHY and 3-trio C-PHY, or 2 × 2-lane D-PHY and 2 × 4-lane D-PHY
Face Detection and Visual Tracking	FDVT	Yes
JPEG Encoder	JPEG	Baseline encoding
Video		
Video Encoder	VENC	H.264, 1080p @ 30fps
Video Decoder	VDEC	H.264/HEVC, 1080p @ 30fps
Audio		
Inter-IC Sound	I2S0	Master/slave receive
	I2S1	Master transmit
	I2S2	Master receive (2 stereo channels)
	I2S3	Master transmit
	I2S5	Master transmit
Pulse Code Modulation	PCM	2(2)
Pulse Density Modulation (decoder for DMIC)	PDM	1
Time Division Multiplexed Interface	TDM	8-channel TX
Analog Baseband	ABB	Yes
Connectivity		
Inter-Integrated Circuit	I2C	9(3)
Universal Asynchronous Receiver/Transmitter	UART	2
Serial Peripheral Interface	SPI	6 (master mode only)
SuperSpeed Universal Serial Bus	SSUSB	SSUSB device or USB 2.0 OTG
KeyPad Scanner	KeyPad	3 × 3
General Purpose I/O pins	GPIO	180

Feature		MT8385
Pulse Width Modulation	PWM	Up to 3
Wireless Connectivity		
Wireless Communication Module (WCM)	WLAN	Dual band: 2.4 GHz and 5 GHz
	BT	Bluetooth 4.2
	GNSS	Yes
	FMSYS	Yes
Miscellaneous		
JTAG® Interface	JTAG	Yes
PMIC Interface	PWRAP	Yes
Auxiliary ADC	AUXADC	12-bit, 5 inputs
Timers	GPT	5 × 32-bit and 1 × 64-bit
	SYSTMR	64-bit
	WDT(4)	Yes

1. DPI pins shared with DBI.
2. PCM merged with I2S.
3. I2C1, I2C2, and I2C4 support MIPI I3C® SDR mode only.
4. The Watchdog Timer (WDT) is part of the Top Reset Generation Unit (TOPRGU).

1.2 Ordering Information

Table 1-2 shows the available ordering part numbers.

Table 1-2 Ordering Information

Part Number	Package	Operational Temperature Range
MT8385V/AZA	VFBGA	See Table 5-3 Recommended Operating Conditions

2 Preface

2.1 Pin Characteristics and Signal Descriptions Conventions

Table 2-1 describes the column headers in all Pin Characteristic and Signal Description tables in Section 4.2 Pin Characteristics and Section 3 Features Description.

Table 2-1 Column Headers Description

Column Name	Explanations
Ball Name	Logical name of the ball. Note that there may exist a selection of several signals for the same ball (aux mode).
Ball Location	Ball's physical location on the chip package
Signal Name	The name of the signal for the given aux mode
Type	Pin type when configured for the given aux mode: • AI: Analog input • AO: Analog output • AIO: Analog bi-directional pin • DI: Digital input • DO: Digital output • DIO: Digital bi-directional pin • P: Power • G: Ground
Description	Description of the signal
Aux. Function	Auxiliary function mode number: • 0 through 7 are possible alternative functions • An empty box means Not Applicable and the ball is dedicated to one function only
Reset State	Shows the Aux. function configured at the release of the SYSRSTB signal
Buffer Type	Describes the associated input/output buffer type
Power Domain	Indicates the voltage supply that powers the terminal IO buffers
PU/PD	Indicates the state of an internal pull-up or pull-down resistor at the release of the SYSRSTB signal: • OFF: Internal pull-up and pull-down are disabled • PU: Pull-up is enabled • PD: Pull-down is enabled • No: Pull-up and Pull-down not available • Blank cell means "No"
IO Reset Value	Shows the IO state at the release of the SYSRSTB signal

2.2 Timing Conventions, Parameters, and Information

This section provides a general description of used symbols, adopted standards and terminology, and test process. All timing characteristics are valid over the represented operating conditions unless otherwise specified.

The interface clock frequency documented in this datasheet is the maximum clock frequency, which corresponds to the maximum programmable frequency on the particular output clock. The frequency defines the maximum limit supported by the device and does not consider into account any system limitation (layouts, connectors, and so forth).

The system designer should take into account these system considerations and the device timing characteristics as well and should determine properly the maximum frequency supported to transfer the data on the corresponding interface.

The timing parameter values do not include delays by board routes. Timing values may be adjusted by increasing/decreasing such delays. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

2.2.1 Timing Parameters and Information

Table 2-2 represents timing parameter symbols and descriptions used in the timing characteristic tables.

Table 2-2 Timing Parameters

Symbol	Description
f_{op}	Operating frequency
t_p	Period (cycle time)
t_d	Delay time
t_{dis}	Disable time
t_{en}	Enable time
t_h	Hold time
t_{su}	Setup time
Start	Start bit
t_t	Transition time
t_v	Valid time
t_w	Pulse duration
t_{FALL}	Fall time
t_{RISE}	Rise time
V_{OH}	High level output voltage
V_{OL}	Low level output voltage
V_{IH}	High level input voltage
V_{IL}	Low level input voltage
V_{REF}	Reference voltage

2.2.2 Parameter Information

This datasheet provides timing values at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be also taken into account.

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

All rise and fall transition timing parameters are referenced correspondingly to 90% and 10% of the signal logical levels, unless otherwise specified.

2.3 Abbreviations

3

3GPP
3rd Generation Partnership Project

A

A-GPS
Assisted GPS
ABB
Analog Baseband
AFBC
Arm Frame Buffer Compression
AI
Artificial Intelligence
APB
Advanced Peripheral Bus
API
Application Programming Interface
AXI
Advanced eXtensible Interface

B

BL
Burst Length
BLE
Bluetoot Low Energy
bps
Bits per Second
BT
Bluetooth Interface

C

CABC
Content Adaptive Backlight Control
CCK
Complementary Code Keying
CDM
Charged Device Model
CLK
Clock
CMDQ
Command Queue
CPHA
Clock Phase
CPOL

Clock Polarity

CPU

Central Processor Unit

CRC

Cyclic Redundancy Check

CS

Chip Select

CSI

Camera Serial Interface

CV

Computer Vision

D

DE

Data Enable

DISP

Display Data Path (Display Controller)

DISP_AAL

Display Adaptive Ambient Light

DISP_CCORR

Display Color Correction

DISP_DITHER

Display Dither

DISP_GAMMA

Display GAMMA

DISP_MUTEX

Display MUTEX

DISP_OVL

Display Overlay

DISP_PWM

Display Pulse Width Modulation

DISP_RDMA

Display Data Path Read DMA

DISP_RSZ

Display Resizer

DISP_WDMA

Display Write Direct Memory Access

DL

Downlink

DMA

Direct Memory Access

DMEM

Data Memory

DPI

Display Parallel Interface

DQS

Data Strobe

DRAM

Dynamic Random Access Memory

DRE

Dark Region Enhancement

DSI

Display Serial Interface

DVFS

Dynamic Voltage and Frequency Scaling

E

EAV

End of Active Video

ECC

Error Checking and Correcting

EMI

External Memory Interface

EPO

Extended Prediction Orbit

F

FD

Face Detection

FIFO

First In First Out

FIR

Finite Impulse Response

FM

Frequency Modulation

FMSYS

Frequency Modulation System

fps

Frames Per Second

G

GIC

Generic Interrupt Controller

GNSS

Global Navigation Satellite System

GPIO

General-Purpose Input/Output

GPS

Global Positioning System

GPU

Graphics Accelerator (Graphics Processing Unit)

H

HBM

Human Body Model

HDMI

High Definition Multimedia Interface

HEVC

High Efficiency Video Coding

HS

High-Speed

HW

Hardware

I

IP

Internet Protocol

ISP

Image Signal Processor

J

JTAG

Joint Test Action Group

L

LCM

Liquid Crystal Monitor

LDO

Low Dropout

LFSR

Linear Feedback Shift Register

LP

Low-power

LPF

Low-Pass Filter

LSB

Least Significant Bit

LTE

Long-Term Evolution

LVDS

Low-Voltage Differential Signaling

M

MACs

Multiply-Accumulate operations

MCDI

Multi-Core Deep Idle

MCLK

Master Clock

MCS

Modulation and Coding Set

MCUSYS

Microcontroller Unit System

MDP

Multimedia Data Path

MDP_CCORR

Multimedia Data Path Color Correction

MDP_RDMA

Multimedia Data Path Read DMA

MDP_TDSHP

Multimedia Data Path 2D Sharpness

MDP_WROT

Multimedia Data Path Rotation

MHL

Mobile High-Definition Link

MISO

Master Input to Slave Output

MMU

Memory Management Unit

MOSI

Master Output to Slave Input

mSBC

modified Sub-Band Codec

MSDC

MMC and SD Controller

MUX

Multiplexer

O

OFDM

Orthogonal Frequency Division Multiplexing

OTG

On-The-Go

OVL

Overlay

P

PA

Power Ampilifier

PBC

Peaking by Color

PCB

Printed Circuit Board

PCM

Pulse Code Modulation

PCO

Phased Coexistence Operation

PDM

Pulse Density Modulation

PIO

Programmed Input/Output

PLC

Packet Loss Concealment

PSMP

Power-Save Multi-Poll

PVT

Process, Voltage and Temperature

PWM

Pulse Width Modulation

PWRAP

PMIC Wrapper

Q

QoS

Quality of Service

R

RBDS

Radio Broadcast Data System

RDMA

Read Direct Memory Access

RDS

Radio Data System

RF

Radio Frequency

RH

Relative Humidity

RIFS

Reduced Interframe Space

ROI

Region-of-Interest

RSZ

Resizer

RX

Receiver

S

SAR

Successive Approximation Register

SAV

Start of Active Video

SBAS

Satellite-Based Augmentation Systems

SBC

Sub-Band Codec

SCCB

Serial Camera Control Bus

SCK

Serial Clock

SCPSYS

System Companion Processor and System Power Manager

SIMD

Single Instruction Multiple Data

SPI

Serial Peripheral Interface

SPM

System Power Management

STBC

Space-Time Block Coding

SW

Software

T

TCP

Transmission Control Protocol

TCXO

Temperature-Compensated Crystal Oscillator

TDM

Time-Division Multiplexing

TE

Tearing Effect

TLB

Translation Lookaside Buffer

TMS

Thermistor Crystal

TOPRGU

Top Reset Generation Unit

TSENSE

Temperature Sensor

TX

Transmitter

U

UART

Universal Asynchronous Receiver/Transmitter

UDP

User Datagram Protocol

UI

Unit Interval

UL

Uplink

USB

Universal Serial Bus

UTMI

USB Transceiver Macrocell Interface

V

VCXO

Voltage Controlled Crystal Oscillator

VDEC

Video Decoder

VENC

Video Encoder

VSYNC

Vertical Synchronization

W

WBG

Wi-Fi, Bluetooth, and GNSS

WDMA

Write DMA

WDT

Watchdog Timer

WMT

Wireless Management Task

WoWLAN

Wake on Wireless LAN

X

xHCI

eXtensible Host Controller Interface

3 Features Description

The MT8385 architecture is a highly integrated and powerful IoT platform incorporating application processing, Visual Processor Unit (VPU), and connectivity subsystems to enable wide range of use cases that require high performance edge processing, advanced multimedia and connectivity capabilities, and high resolution cameras. The platform features advanced implementation of Quad-core Arm Cortex-A73 and Cortex-A53, both operating at up to 2.0 GHz, and powerful graphics accelerator. The MT8385 features LPDDR3 and LPDDR4/X for optimal performance and also supports booting from eMMC to minimize the overall BOM cost. In addition, an extensive set of interfaces is included to connect to cameras, touch screen displays, and MMC™/SD cards.

The Quad-core Arm Cortex-A73 and Cortex-A53 equipped with Arm Neon™ engine, offer necessary processing power to support the latest high level operating systems along with demanding applications such as web browsing, email, GPS navigation and games. This content can be enhanced by the 2D/3D graphics accelerator and then visualized on a high resolution touch screen display. To provide advanced multimedia applications and services such as streaming audio and video, the device features a multi-standard video accelerator with a multitude of decoders and encoders such as HEVC and H.264, and an advanced audio subsystem.

The integrated VPU core enables deep learning, neural network acceleration, and computer vision applications. The latter, combined with the up to 32MP camera, can clearly and accurately perform AI-vision functions such as facial recognition, object identification, scene analysis, optical character recognition and much more.

Through a single antenna shared with the external MT7668/MT6631 connectivity chip, the device provides the most convenient solution in the industry. With its small footprint and low power consumption it enables a wide variety of potential device designs, reducing development costs and accelerating time to market.

3.1 Application Processors

The device includes an Arm-based processor subsystem (MCUSYS), which is responsible for running operating system and application programs in the device. It comprises of two different CPU clusters providing different levels of power efficiency and computing power to satisfy a wide range of system power and performance requirements. The power efficiency of Cluster 0 (Quad-core Arm Cortex-A53 processor) is specially optimized to minimize the power consumption in daily usage scenarios and lightweight applications. For more computing intensive and latency sensitive workloads, Cluster 1 (Quad-core Arm Cortex-A73 processor) can provide higher performance level with reasonable power consumption.

The MCUSYS also includes the Arm GIC-500 interrupt controller that provides interrupt support for both Arm clusters.

The MCUSYS supports Dynamic Voltage and Frequency Scaling (DVFS) technology which allows the CPU to run at different frequency and voltage configurations for different application requirements. Besides DVFS, the power of each CPU core can be turned off individually when not used. In standby mode, the MCUSYS can be completely shut down to further reduce power consumption and optimize the battery usage on mobile devices.

3.1.1 Cortex-A73 Processor

The A73 cluster supports the following key features:

- Quad-core implementation
- Neon processing engine with SIMDv2/VFPv4 ISA
- Full compliance with Armv8-A architecture:
  - AArch32 and AArch64 execution states at all Exception Levels (EL0 to EL3)

  - A64 instruction set
  - A32 instruction set (Arm instruction set in pre-Armv8 architectures)
  - T32 instruction set (Arm Thumb® instruction set in pre-Armv8 architectures)
- Arm Jazelle® technology
- In-order pipeline with direct and indirect branch prediction
- Generic timers supporting 64-bit count input from SYSTMR
- Level 1 (L1) and Level 2 (L2) cache memory with cache line length of 64 bytes:
  - 64KB L1 instruction cache (L1I)
  - 64KB L1 data cache (L1D)
  - 1024KB unified L2 cache
- Memory Management Unit (MMU):
  - 32-entry, fully-associative, L1 instruction micro Translation Lookaside Buffer (TLB)
  - 48-entry, fully-associative, L1 data micro TLB
  - A main TLB which contains two cache RAMs accessed in parallel:
    - 4-way, set-associative, 1024-entry cache which stores virtual address (VA) to physical address (PA) mappings for smaller page sizes (4KB, 16KB, 64KB)
    - 2-way, set-associative, 128-entry cache which stores virtual address (VA) to physical address (PA) mappings for larger page sizes (1MB, 2MB, 16MB, 32MB, 512MB, 1GB)
- Security:
  - TrustZone®
  - Secure boot (refer to Section 3.15 Boot Modes)
- Debug:
  - Armv8 debug logic
  - Arm CoreSight™ architecture
- 128-bit AXI master interface—directly connected to External Memory Interface (EMI) to minimize the access latency to DRAM thus providing sufficient memory bandwidth

3.1.2 Cortex-A53 Processor

The A53 cluster supports the following key features:

- Quad-core implementation
- Neon processing engine with SIMDv2/VFPv4 ISA
- Full compliance with Armv8-A architecture:
  - AArch32 and AArch64 execution states at all Exception Levels (EL0 to EL3)
  - A64 instruction set
  - A32 instruction set (Arm instruction set in pre-Armv8 architectures)
  - T32 instruction set (Arm Thumb instruction set in pre-Armv8 architectures)
- Arm Jazelle technology
- In-order pipeline with direct and indirect branch prediction
- Generic timers supporting 64-bit count input from SYSTMR
- Level 1 (L1) and Level 2 (L2) cache memory with cache line length of 64 bytes:
  - 32KB L1 instruction cache (L1I)
  - 32KB L1 data cache (L1D)
  - 1024KB unified L2 cache
- Memory Management Unit (MMU):
  - 10-entry, fully-associative, L1 instruction micro Translation Lookaside Buffer (TLB)
  - 10-entry, fully-associative, L1 data micro TLB

  - 4-way, set-associative, 512-entry unified main TLB
- Security:
  - TrustZone
  - Secure boot (refer to Section 3.15 Boot Modes)
- Debug:
  - Armv8 debug logic
  - Arm CoreSight architecture
- 128-bit AXI master interface—directly connected to External Memory Interface (EMI) to minimize the access latency to DRAM thus providing sufficient memory bandwidth

3.2 Graphics Accelerator

The device Graphics Accelerator (GPU) is based on Arm Mali-G72 MP3 core. It is used to process extremely complicated graphics and perform general processing tasks assigned by the main application processor.

The GPU supports the following key features:

- An enhanced API feature set with high-performance support for both shader-based and fixed-function graphics APIs. The supported API graphics industry standards are:
  - OpenGL ES 1.1, 2.0, 3.0, 3.1, 3.2
  - DirectX® 9, 11.1, 12
  - Vulkan 1.0
  - OpenCL 1.0, 1.1, 1.2, 2.0
- Anti-aliasing capabilities
- An effective core for General-Purpose computing on GPU (GPGPU) applications
- High memory bandwidth and low-power consumption for 3-Dimensional (3D) graphics content
- Arm Frame Buffer Compression (AFBC) and compressed texture formats
- 10- and 16-bit YUV input and output formats
- Bus protocol:
  - One 128-bit master AXI4 bus, with support of 64 read and 32 write outstanding transactions
  - One 32-bit slave AXI4 bus
- 256KB L2 cache (4-way, set-associative)

3.3 System Companion Processor

The System Companion Processor (SCP) is a processor subsystem that includes an Arm Cortex-M4 processor and a variety of peripherals. The special design of the SCP makes it suitable for running applications such as Voice Wakeup, Sensor HUB and future tasks when the entire device is in suspend mode. The SCP is connected to infra bus and therefore can access DRAM, audio SRAM and other hardware resources through this bus.

The SCP includes the following key features:

- Up to 512KB Tightly Coupled Memory (TCM)
- An AHB interface for device memory and register access
- An AHB interface for audio memory and register access
- An APB interface for MCUSYS configuration
- Interprocessor interrupt to MCUSYS
- Serial audio interface to support Voice Wakeup
- 6 × 32-bit down-count timers with selectable clock source
- Interrupt controller

- Support of 12-input external interrupt with debounce function
- 2 × I2C
- 3 × SPI
- 2 × UART
- 8-bit GPIO
- Direct path to PMIC wrapper
- Watchdog timer

3.3.1 SCP Signal Descriptions

Table 3-1 presents SCP signal descriptions.

Table 3-1 SCP Signal Descriptions

Signal Name	Type	Description	Ball Location
SCP_SPI0			
SCP_SPI0_CK	DO	SCP SPI0 serial clock	AF3
SCP_SPI0_CS	DO	SCP SPI0 chip select	AG3
SCP_SPI0_MI	DI	SCP SPI0 master input / slave output	AJ2
SCP_SPI0_MO	DO	SCP SPI0 master output / slave input	AH2
SCP_SPI1			
SCP_SPI1_CK	DO	SCP SPI1 serial clock	AA22
SCP_SPI1_CS	DO	SCP SPI1 chip select	AB25
SCP_SPI1_MI	DI	SCP SPI1 master input / slave output	W22
SCP_SPI1_MO	DO	SCP SPI1 master output / slave input	Y22
SCP_SPI2			
SCP_SPI2_CK	DO	SCP SPI2 serial clock	AG2
SCP_SPI2_CS	DO	SCP SPI2 chip select	AB5
SCP_SPI2_MI	DI	SCP SPI2 master input / slave output	AE3
SCP_SPI2_MO	DO	SCP SPI2 master output / slave input	AB4
SCP Command signals			
SCP_VREQ_VAO	DO	SCP to PMIC normal voltage request	AG1, AB23, AA6, L4, N25, Y25

3.4 Vision Processor Unit

The Vision Processor Unit (VPU) is a highly efficient computing processor that is best suited for Artificial Intelligence (AI) and Computer Vision (CV) algorithms. The VPU is composed of two Cadence Vision P6 (VP6) cores sharing a common local interconnect network.

Each VP6 core supports the following key features:

- Support of iDMA for data transfer between VP6 internal Data Memory (DMEM) and external DRAM
- L1 instruction memory:
  - 192KB instruction RAM
  - 128KB instruction cache
- L1 data memory:
  - 256KB data RAM (2 banks, 128KB per bank)
  - 16KB data cache
- Top performance:

  - CV + AI up to 256 GMAC/sec
- Number of MACs per cycle:
  - 256 × 8x8 MACs
  - 128 × 8x16 MACs
  - 64 × 16x16 MACs
- Histogram package
- Scatter/Gather engine (8 × sub-banks)

3.5 Memory

The device connects to external memories using External Memory Interface (EMI) controller and Dynamic Random-Access Memory Controller (DRAMC) with DDR PHY. EMI is a sophisticated communication interface between external memories and the device.

The EMI controller processes requests from the device masters and issues commands to the DRMAC. It has the following key features:

- Prevents DRAM stall, data overflow, and underflow
- Allows gating its own clock when idle
- Performance monitoring
- Connection to two DRAMCs
- Command schedule options:
  - Starvation control
  - Bandwidth limiter
  - Priority control
  - Page hit control
  - Read and write turn around prevent control
- Dedicated AXI connection ports:
  - 2 × 128-bit read and write ports to the MCUSYS
  - 2 × 128-bit read and write ports to the multimedia modules
  - 2 × 128-bit read and write ports to the GPU system

Each DRAMC processes EMI commands and controls the external memory. It has the following key features:

- Contains integrated DDR PHY
- Supports the following DDR memory types:
  - 32-bit LPDDR3 at 1866 MT/s
  - 16-bit LPDDR4/X at 3733 MT/s (eMCP package) or 3200 MT/s (discrete package)
- Schedules and issues DRAM bus commands
- Keeps the integrity of DRAM bus timings
- Burst Length (BL) support: BL4, BL8
- Support of maximum 8GB LPDDR4/X device
- Supports power-down and self-refresh
- Supports clock stop
- Support of input DQS/DQ timing calibration for PVT variation
- Supports read/write command out of order control
- Supports LPDDR4 byte mode
- Supports per-bank refresh

3.5.1 EMI Signal Descriptions

Table 3-2 presents EMI signal descriptions.

Table 3-2 EMI Signal Descriptions (LPDDR4)

Signal Name	Type	Description	Ball Location
EMI_EXTR(1)	DIO	DRAM output driving calibration resistor	A2
EMI_RESET_N	DIO	DRAM reset output	D22
EMI_TN	DIO	Not used. Leave unconnected.	J14
EMI_TP(2)	DIO	DRAM voltage reference 2, connected to ½ AVDDQ_EMI0	J15
EMI0 Address Bus—EMI0_CA[5:0]			
EMI0_CA0	DIO	DRAM address output 0	E9
EMI0_CA1	DIO	DRAM address output 1	C7
EMI0_CA2	DIO	DRAM address output 2	B5
EMI0_CA3	DIO	DRAM address output 3	B6
EMI0_CA4	DIO	DRAM address output 4	B7
EMI0_CA5	DIO	DRAM address output 5	E7
EMI0 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI0_CK_C	DIO	DRAM clock 0 output	E10
EMI0_CK_T	DIO	DRAM clock 0 output	D10
EMI0_CKE0	DIO	DRAM command output clock enable 0	E8
EMI0_CKE1	DIO	DRAM command output clock enable 1	D7
EMI0_CS0	DIO	DRAM chip select 0	D8
EMI0_CS1	DIO	DRAM chip select 1	A7
EMI0_DMI0	DIO	DRAM DQM 0	B4
EMI0_DMI1	DIO	DRAM DQM 1	C8
EMI0_DQS0_C	DIO	DRAM DQS 0	C4
EMI0_DQS0_T	DIO	DRAM DQS 0	D4
EMI0_DQS1_C	DIO	DRAM DQS 1	E12
EMI0_DQS1_T	DIO	DRAM DQS 1	F12
EMI0 Data Bus—EMI0_DQ[15:0]			
EMI0_DQ0	DIO	DRAM data pin 0	E5
EMI0_DQ1	DIO	DRAM data pin 1	D5
EMI0_DQ2	DIO	DRAM data pin 2	E6
EMI0_DQ3	DIO	DRAM data pin 3	D6
EMI0_DQ4	DIO	DRAM data pin 4	B3
EMI0_DQ5	DIO	DRAM data pin 5	C5
EMI0_DQ6	DIO	DRAM data pin 6	A5
EMI0_DQ7	DIO	DRAM data pin 7	A3
EMI0_DQ8	DIO	DRAM data pin 8	B11
EMI0_DQ9	DIO	DRAM data pin 9	E11
EMI0_DQ10	DIO	DRAM data pin 10	B10
EMI0_DQ11	DIO	DRAM data pin 11	A9
EMI0_DQ12	DIO	DRAM data pin 12	A11
EMI0_DQ13	DIO	DRAM data pin 13	D9
EMI0_DQ14	DIO	DRAM data pin 14	C9
EMI0_DQ15	DIO	DRAM data pin 15	D11

Signal Name	Type	Description	Ball Location
EMI1 Address Bus—EMI1_CA[5:0]			
EMI1_CA0	DIO	DRAM address output 0	D17
EMI1_CA1	DIO	DRAM address output 1	C15
EMI1_CA2	DIO	DRAM address output 2	B17
EMI1_CA3	DIO	DRAM address output 3	A17
EMI1_CA4	DIO	DRAM address output 4	C17
EMI1_CA5	DIO	DRAM address output 5	D19
EMI1 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI1_CK_C	DIO	DRAM clock 0 output	F16
EMI1_CK_T	DIO	DRAM clock 0 output	E16
EMI1_CKE0	DIO	DRAM command output clock enable 0	D18
EMI1_CKE1	DIO	DRAM command output clock enable 1	E18
EMI1_CS0	DIO	DRAM chip select 0	E17
EMI1_CS1	DIO	DRAM chip select 1	C16
EMI1_DMI0	DIO	DRAM DQM 0	B18
EMI1_DMI1	DIO	DRAM DQM 1	B15
EMI1_DQS0_C	DIO	DRAM DQS 0	E21
EMI1_DQS0_T	DIO	DRAM DQS 0	F21
EMI1_DQS1_C	DIO	DRAM DQS 1	F13
EMI1_DQS1_T	DIO	DRAM DQS 1	E13
EMI1 Data Bus—EMI1_DQ[15:0]			
EMI1_DQ0	DIO	DRAM data pin 0	F20
EMI1_DQ1	DIO	DRAM data pin 1	E20
EMI1_DQ2	DIO	DRAM data pin 2	D20
EMI1_DQ3	DIO	DRAM data pin 3	E19
EMI1_DQ4	DIO	DRAM data pin 4	C20
EMI1_DQ5	DIO	DRAM data pin 5	B19
EMI1_DQ6	DIO	DRAM data pin 6	A19
EMI1_DQ7	DIO	DRAM data pin 7	C21
EMI1_DQ8	DIO	DRAM data pin 8	C13
EMI1_DQ9	DIO	DRAM data pin 9	C14
EMI1_DQ10	DIO	DRAM data pin 10	A13
EMI1_DQ11	DIO	DRAM data pin 11	D15
EMI1_DQ12	DIO	DRAM data pin 12	C12
EMI1_DQ13	DIO	DRAM data pin 13	A15
EMI1_DQ14	DIO	DRAM data pin 14	B14
EMI1_DQ15	DIO	DRAM data pin 15	D14

1. Connect this pin through an external resistor to GND. An external voltage should be applied.
2. This pin should be connected via 100-nF capacitors to the corresponding EMI power supply and GND. If not used, it can be left unconnected.

3.5.2 EMI Signal Mapping

Table 3-3 presents EMI signals mapping per device memory type.

Table 3-3 EMI Signals Mapping (LPDDR4 to LPDDR3)

Ball Location	Ball Name	Pin-Mux 1 - LPDDR4 2 × 16-bit	Pin-Mux 2 - LPDDR3 1 × 32-bit
E5	EMI0_DQ0	DQ0	CA9
D5	EMI0_DQ1	DQ1	NC
E6	EMI0_DQ2	DQ2	CA8
D6	EMI0_DQ3	DQ3	CA5
B3	EMI0_DQ4	DQ4	CA7
C5	EMI0_DQ5	DQ5	CA2
A5	EMI0_DQ6	DQ6	CA6
A3	EMI0_DQ7	DQ7	CA6
B11	EMI0_DQ8	DQ8	DQ22
E11	EMI0_DQ9	DQ9	DQ23
B10	EMI0_DQ10	DQ10	DQ20
A9	EMI0_DQ11	DQ11	DQ19
A11	EMI0_DQ12	DQ12	DQ12
D9	EMI0_DQ13	DQ13	DQ13
C9	EMI0_DQ14	DQ14	DQ14
D11	EMI0_DQ15	DQ15	DQ15
C4	EMI0_DQS0_C	DQS0_c	NC
D4	EMI0_DQS0_T	DQS0_t	NC
E12	EMI0_DQS1_C	DQS1_c	DQS2_c
F12	EMI0_DQS1_T	DQS1_t	DQS2_t
E9	EMI0_CA0	CA0	CA0
C7	EMI0_CA1	CA1	CA1
B5	EMI0_CA2	CA2	CA3
B6	EMI0_CA3	CA3	NC
B7	EMI0_CA4	CA4	NC
E7	EMI0_CA5	CA5	NC
D8	EMI0_CS0	CS0	CS0
A7	EMI0_CS1	CS1	CS1
B4	EMI0_DMI0	DM0	NC
C8	EMI0_DMI1	DM1	DM2
E8	EMI0_CKE0	CKE0	CKE0
D7	EMI0_CKE1	CKE1	CKE1
E10	EMI0_CK_C	CK_c	CK_c
D10	EMI0_CK_T	CK_t	CK_t
F20	EMI1_DQ0	DQ0	DQ26
E20	EMI1_DQ1	DQ1	DQ27
D20	EMI1_DQ2	DQ2	DQ24
E19	EMI1_DQ3	DQ3	DQ25
C20	EMI1_DQ4	DQ4	DQ30
B19	EMI1_DQ5	DQ5	DQ28

Ball Location	Ball Name	Pin-Mux 1 - LPDDR4 2 × 16-bit	Pin-Mux 2 - LPDDR3 1 × 32-bit
A19	EMI1_DQ6	DQ6	DQ31
C21	EMI1_DQ7	DQ7	DQ29
C13	EMI1_DQ8	DQ8	DQ2
C14	EMI1_DQ9	DQ9	DQ4
A13	EMI1_DQ10	DQ10	DQ1
D15	EMI1_DQ11	DQ11	DQ6
C12	EMI1_DQ12	DQ12	DQ0
A15	EMI1_DQ13	DQ13	DQ7
B14	EMI1_DQ14	DQ14	DQ3
D14	EMI1_DQ15	DQ15	DQ5
E21	EMI1_DQS0_C	DQS0_c	DQS3_c
F21	EMI1_DQS0_T	DQS0_t	DQS3_t
F13	EMI1_DQS1_C	DQS1_c	DQS0_c
E13	EMI1_DQS1_T	DQS1_t	DQS0_t
D17	EMI1_CA0	CA0	DQ11
C15	EMI1_CA1	CA1	DQ8
B17	EMI1_CA2	CA2	DQ15
A17	EMI1_CA3	CA3	DQ14
C17	EMI1_CA4	CA4	DQ9
D19	EMI1_CA5	CA5	DQ13
E17	EMI1_CS0	CS0	DM1
C16	EMI1_CS1	CS1	NC
B18	EMI1_DMI0	DM0	DM3
B15	EMI1_DMI1	DM1	DM0
D18	EMI1_CKE0	CKE0	DQ10
E18	EMI1_CKE1	CKE1	DQ12
F16	EMI1_CK_C	CK_C	DQS1_c
E16	EMI1_CK_T	CK_T	DQS1_t
D22	EMI_RESET_N	RESET_N	RESET_N
J15	EMI_TP	NC	VREF
J14	EMI_TN	NC	NC
A2	EMI_EXTR	EXTR	EXTR

3.5.3 LPDDR3 Interface

3.5.3.1 LPDDR3 Timing Characteristics

The EMI LPDDR3 timing characteristics are compliant with JEDEC Standard—JESD209-3C.

3.5.3.2 LPDDR3 Application Guidelines

Table 3-4 presents supported LPDDR3 device combinations.

Table 3-4 LPDDR3 Device Combinations

Number of Devices	Device Data Width	Mirrored	EMI Width
1	32-bit	No	32-bit

Figure 3-1 shows the schematic connections for a 32-bit interface using 1 × 32-bit device.

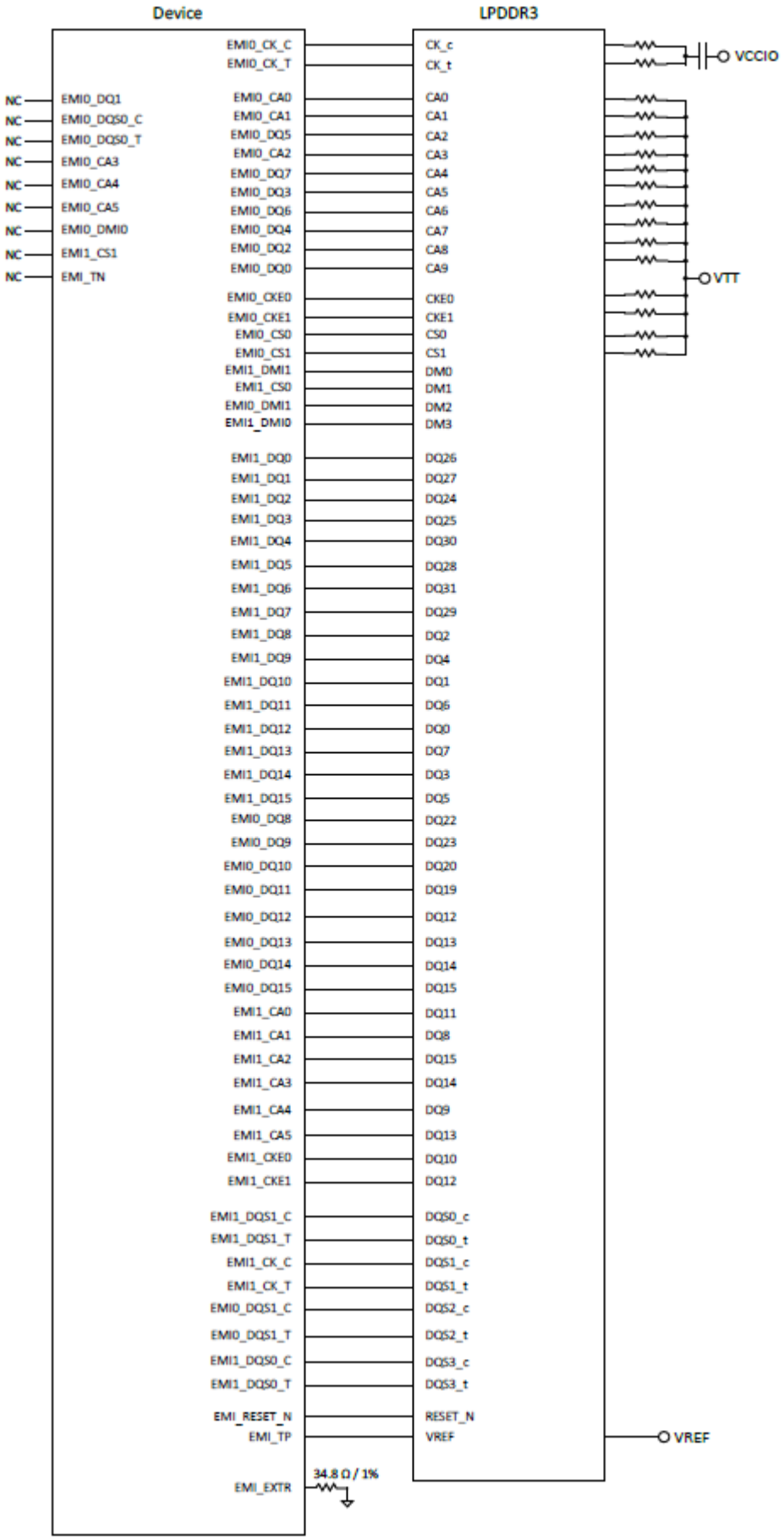


Figure 3-1 LPDDR3 Basic Schematic for 1 × 32-bit

3.5.4 LPDDR4/X Interface

3.5.4.1 LPDDR4/X Timing Characteristics

The EMI LPDDR4 timing characteristics are compliant with JEDEC Standard—JC-42.6.

3.5.4.2 LPDDR4/X Application Guidelines

Table 3-5 presents supported LPDDR4/X device combinations.

Table 3-5 LPDDR4/X Device Combinations

Number of Devices	Device Data Width	Mirrored	EMI Width
2	16-bit	No	32-bit

Figure 3-2 shows the schematic connections for a 32-bit interface using 2 × 16-bit devices.

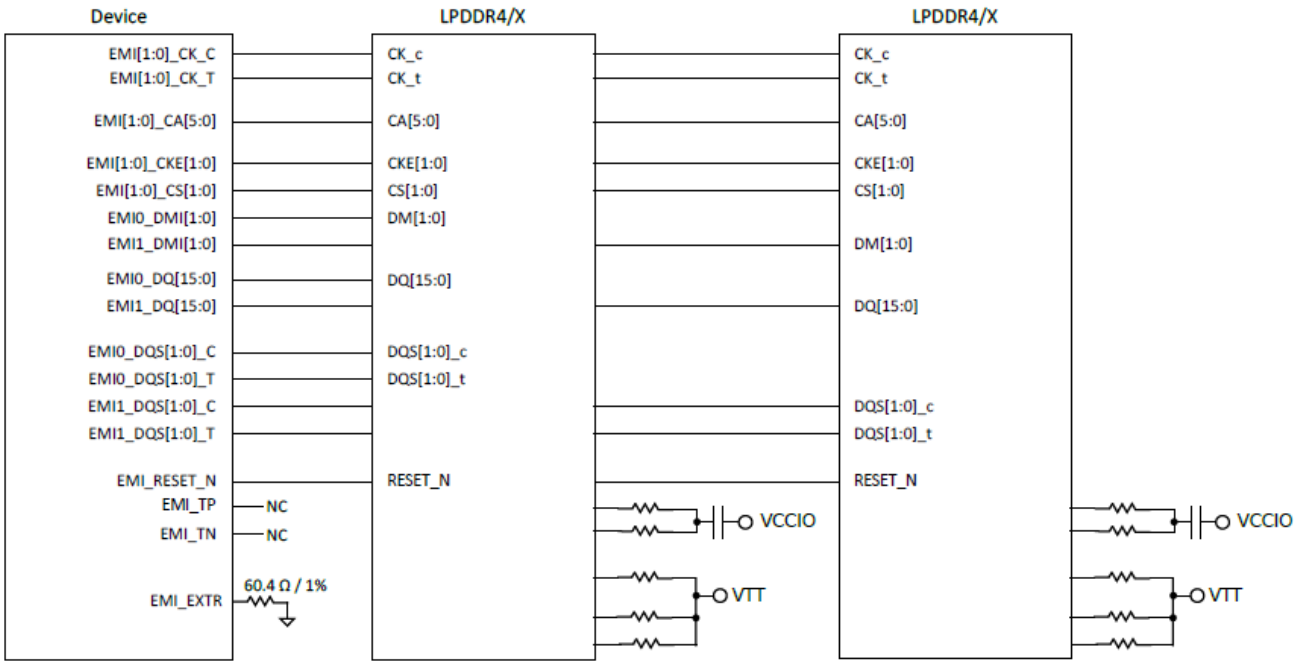


Figure 3-2 LPDDR4/X Basic Schematic for 2 × 16-bit

3.6 Storage

3.6.1 Memory Card Controller (MSDC)

The MultiMediaCard and Secure Digital® (SD) card Controller (MSDC) offers a high throughput data transfers while power consumption and data security between device local hosts and memory cards are taken into consideration.

The MSDC fully supports:

- SD3.0 (Secure Digital) memory card specification
- eMMC5.1 (embedded MultiMediaCard) specification

The device includes two MSDC modules. MSDC0 is used as MMC/eMMC interface, while MSDC1 is used as SD interface. Each MSDC module supports the following key features:

- Built-in CRC circuit

- Programmed Input/Output (PIO) mode, basic DMA mode and descriptor mode
- Interrupt capabilities

The MSDC0 fully supports:

- 1-, 4-, 8-bit data bus width for eMMC
- Backwards compatibility with legacy MMC card
- High-speed Single Data Rate (SDR) mode
- High-speed Dual Data Rate (DDR) mode
- HS200 mode, SDR up to 200 MBps
- HS400 mode, DDR up to 400 MBps
- eMMC Boot up mode
- eMMC5.1 Command Queue (CMDQ)
- AES

The MSDC1 fully supports:

- 1-, 4-bit data bus width for SD card interface or SDIO interface
- Default Speed mode, data rate up to 12.5 MBps
- High Speed mode, data rate up to 25 MBps
- SDR12 mode, data rate up to 12.5 MBps
- SDR25 mode, data rate up to 25 MBps
- SDR50 mode, data rate up to 50 MBps
- SD3.0 SDR104 mode, data rate up to 100 MBps
- SD3.0 DDR50 mode, data rate up to 50 MBps

3.6.1.1 MSDC Signal Descriptions

Table 3-6 presents MSDC signal descriptions.

Table 3-6 MSDC Signal Descriptions

Signal Name	Type	Description	Ball Location
MSDC0			
MSDC0_CLK	DO	MSDC0 clock output	D24
MSDC0_CMD	DIO	MSDC0 command pin	C27
MSDC0_DAT0	DIO	MSDC0 data 0 pin	B26
MSDC0_DAT1	DIO	MSDC0 data 1 pin	B27
MSDC0_DAT2	DIO	MSDC0 data 2 pin	A26
MSDC0_DAT3	DIO	MSDC0 data 3 pin	E24
MSDC0_DAT4	DIO	MSDC0 data 4 pin	C26
MSDC0_DAT5	DIO	MSDC0 data 5 pin	C25
MSDC0_DAT6	DIO	MSDC0 data 6 pin	G23
MSDC0_DAT7	DIO	MSDC0 data 7 pin	D26
MSDC0_DSL	DI	MSDC0 DSL pin	E25
MSDC0_RSTB	DO	MSDC0 reset pin	D25
MSDC1			
MSDC1_CLK	DO	MSDC1 clock output	AC24
MSDC1_CMD	DIO	MSDC1 command pin	AD26
MSDC1_DAT0	DIO	MSDC1 data 0 pin	AD24

Signal Name	Type	Description	Ball Location
MSDC1_DAT1	DIO	MSDC1 data 1 pin	AE26
MSDC1_DAT2	DIO	MSDC1 data 2 pin	AC23
MSDC1_DAT3	DIO	MSDC1 data 3 pin	AD27

3.6.1.2 MSDC Signal Mapping

The communication protocol between controller and device is implemented through an advanced 11-signal or 6-signal bus. Details are provided in Table 3-7.

Table 3-7 MSDC Signal Mapping

No.	Name(1)(2)	Type	eMMC	SD/SDHC	SDIO	Description
1	MSDC0/1_CLK	DO	CLK	CLK	SCLK	Clock
2	MSDC0_RSTB	DO	RCLK			Reset output
3	MSDC0/1_DAT0	DIO	DAT0	DAT0	DAT0	Serial data line bit 0
4	MSDC0/1_DAT1	DIO	DAT1	DAT1	DAT1	Serial data line bit 1
5	MSDC0/1_DAT2	DIO	DAT2	DAT2	DAT2	Serial data line bit 2
6	MSDC0/1_DAT3	DIO	DAT3	DAT3	DAT3	Serial data line bit 3
7	MSDC0_DAT4	DIO	DAT4			Serial data line bit 4
8	MSDC0_DAT5	DIO	DAT5			Serial data line bit 5
9	MSDC0_DAT6	DIO	DAT6			Serial data line bit 6
10	MSDC0_DAT7	DIO	DAT7			Serial data line bit 7
11	MSDC0/1_CMD	DIO	CMD	CMD	BS	Command/bus state
12	SD_WP(3)	I		WP		Write protection detect
13	SD_INS(3)	I	VSS2	VSS2	INS	Card insertion detect

1. All MSDC I/O pads include both pull-up and pull-down resistors because they are shared by both the Memory Stick and SD/MMC memory card. Pull-down resistor for these pins can be used for power saving.
2. All embedded pull-up and pull-down resistors can be disabled by programming the corresponding control registers if optimal pull-up or pull-down resistors are required on the system board.
3. SD_WP and SD_INS signals are not provided by MSDC controller. These functions can be accomplished using GPIO pins, if needed.

3.6.1.3 MSDC Timing Characteristics

Table 3-8 and Figure 3-3 present the MSDC timing characteristics in Default Speed mode.

Table 3-8 MSDC Timing Characteristics (Default Speed mode)

No	Symbol	Parameter	Min	Max	Unit
Clock CLK (CLK rise and fall times are measured by min V_{IH} and max V_{IL}); C_{CARD} ≤ 10 pF					
DS1	f_{OP}	Operating frequency data transfer mode	0	25	MHz
	f_{OP_ID}	Operating frequency identification mode	100	400	kHz
DS2	$t_{w\_CLK\_L}$	Pulse duration, CLK low	10		ns
DS3	$t_{w\_CLK\_H}$	Pulse duration, CLK high	10		ns
DS4	t_{RISE_CLK}	Rise time, CLK		10	ns
DS5	t_{FALL_CLK}	Fall time, CLK		10	ns
Input DAT/CMD (referenced to CLK); C_{CARD} ≤ 10 pF					
DS6	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input	5		ns
DS7	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input	5		ns

No	Symbol	Parameter	Min	Max	Unit
Output DAT/CMD (referenced to CLK); $C_L \leq 40$ pF					
DS8	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output during data transfer mode	0	14	ns
DS9	t_{d_DAT/CMD_ID}	Delay time, DAT/CMD output during identification mode	0	50	ns

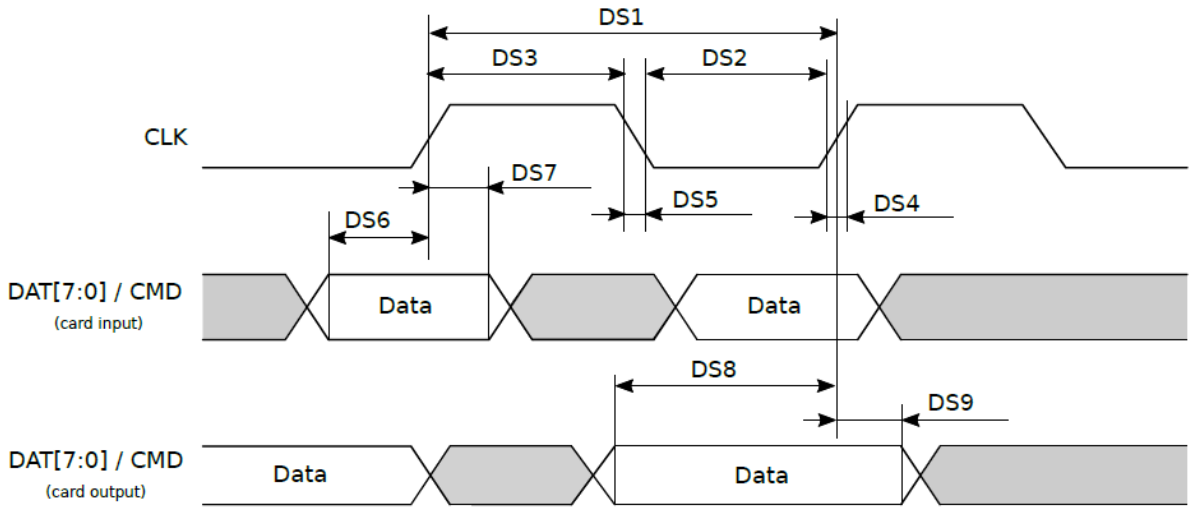


Figure 3-3 MSDC Timing Diagram (Default Speed mode)

Table 3-9 and Figure 3-4 present the MSDC timing characteristics in High Speed mode.

Table 3-9 MSDC Timing Characteristics (High Speed mode)

No	Parameter			Min	Max	Unit
Clock CLK (CLK rise and fall times are measured by min V_{IH} and max V_{IL}); $C_{CARD} \leq 10$ pF						
HS1	f_{OP}	Operating frequency data transfer mode		0	50	MHz
HS2	$t_{w\_CLK\_L}$	Pulse duration, CLK low		7		ns
HS3	$t_{w\_CLK\_H}$	Pulse duration, CLK high		7		ns
HS4	t_{RISE_CLK}	Rise time, CLK			3	ns
HS5	t_{FALL_CLK}	Fall time, CLK			3	ns
Input DAT/CMD (referenced to CLK); $C_{CARD} \leq 10$ pF						
HS6	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input		6		ns
HS7	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input		2		ns
Output DAT/CMD (referenced to CLK)						
HS8	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output (1)	$C_L \leq 40$ pF		14	ns
HS9	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output (1)	$C_L \geq 15$ pF	2.5		ns
	C_L	Total system capacitance for each line			40	pF

1. Valid during data transfer mode.

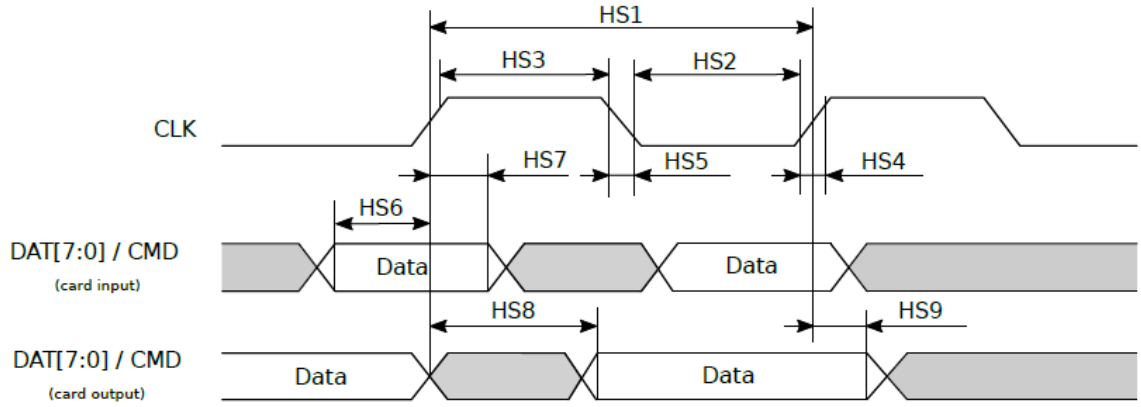


Figure 3-4 MSDC Timing Diagram (High Speed mode)

Table 3-10 and Figure 3-5 present the MSDC timing characteristics in SDR12, SDR25, SDR50, and SDR104 modes.

Table 3-10 MSDC Timing Characteristics (SDR12/SDR25/SDR50/SDR104 modes)

No.	Parameter		Min	Max	Unit
CLK output from host					
SDR121	t_C	Cycle time, CLK for SDR12		40	ns
		Cycle time, CLK for SDR25		20	ns
		Cycle time, CLK for SDR50		10	ns
		Cycle time, CLK for SDR104		4.8	ns
	D	Duty Cycle, CLK	30	70	%
SDR124	t_{RISE_CLK}	Rise time, CLK		0.2 × SDR121(1)	ns
SDR125	t_{FALL_CLK}	Fall time, CLK		0.2 × SDR121(1)	ns
Host DAT/CMD input (referenced to CLK), V_{CT} = 0.975V					
SDR126	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input for SDR50, C_{CARD} = 10 pF	3		ns
		Setup time, DAT/CMD input for SDR104, C_{CARD} = 10 pF	1.4		ns
SDR127	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input for SDR50, C_{CARD} = 5 pF	0.8		ns
		Hold time, DAT/CMD input for SDR104, C_{CARD} = 5 pF	0.8		ns
Host DAT/CMD output (referenced to CLK)					
SDR128	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output for SDR12/SDR25, $t_C \geq 20.0$ ns, C_L = 40 pF, using driver type B		14	ns
		Delay time, DAT/CMD output for SDR50, $t_C \geq 10.0$ ns, C_L = 30 pF, using driver type B		7.5	ns
		Delay time, DAT/CMD output for SDR104	0	2	UI(2)
	$\Delta t_{d\_DAT/CMD}$	Delay variation due to temperature change after tuning for SDR104	-350	+1550	ps
SDR129	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output for SDR12/SDR25/SDR50, C_L = 15 pF	1.5		ns
SDR1210	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output for SDR104	0.6(3)		UI(2)

1. $t_{RISE\_CLK}/t_{FALL\_CLK}$ < 0.96 ns (max) at 208 MHz, C_{CARD} = 10 pF; $t_{RISE\_CLK}/t_{FALL\_CLK}$ < 2 ns (max) at 100 MHz, C_{CARD} = 10 pF.
2. Unit Interval (UI) is one bit nominal time. For example, UI = 5 nsat 200 MHz.

3. $t_{h\_DAT/CMD}$ = 2.88 ns at 208 MHz

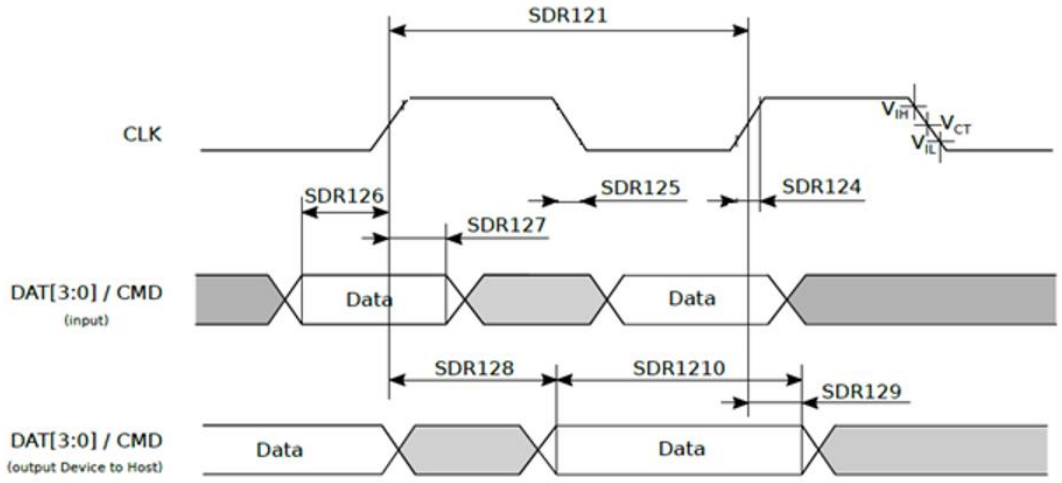


Figure 3-5 MSDC Timing Diagram (SDR12/SDR25/SDR50/SDR104 modes)

Table 3-11 and Figure 3-6 present the MSDC timing characteristics in DDR50 mode.

Table 3-11 MSDC Timing Characteristics (DDR50 mode)

No	Parameter			Min	Max	Unit
Input DAT/CMD (referenced to CLK rising and falling edge / rising edge); C_{CARD} ≤ 10 pF						
DDR503	t_{su_CMD}	Setup time, CMD input		6		ns
	t_{su_DAT}	Setup time, DAT input		3		ns
DDR504	t_{h_CMD}	Hold time, CMD input		0.8		ns
	t_{h_DAT}	Hold time, DAT input		0.8		ns
Output DAT/CMD (referenced to CLK rising and falling edge / rising edge)						
DDR505	t_{d_CMD}	Delay time, CMD output (1)	C_L ≤ 30 pF		13.7	ns
	t_{d_DAT}	Delay time, DAT output (1)	C_L ≤ 25 pF		7	ns
DDR506	t_{h_CMD}	Hold time, CMD output	C_L ≥ 15 pF	1.5		ns
	t_{h_DAT}	Hold time, DAT output	C_L ≥ 15 pF	1.5		ns

1. Valid during data transfer mode.

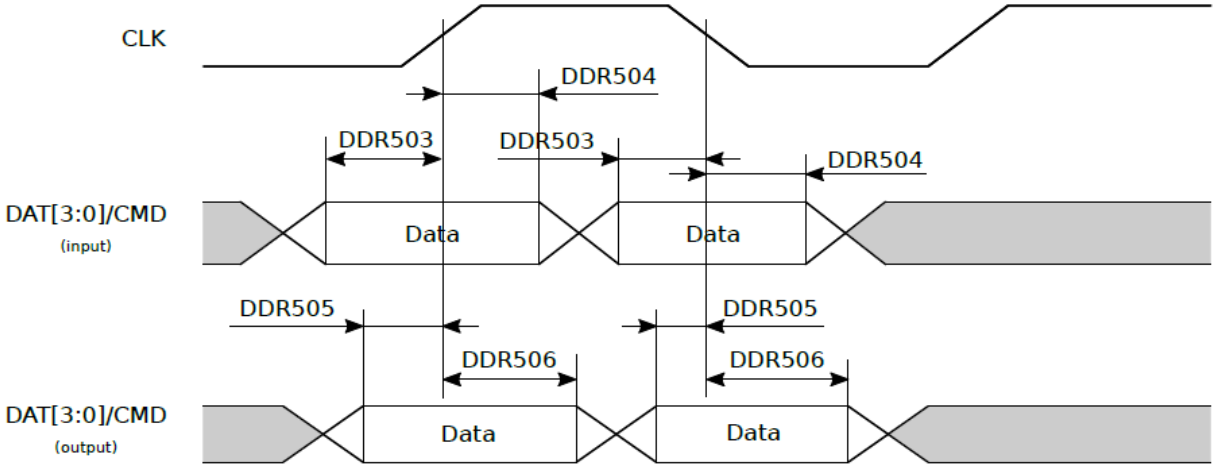


Figure 3-6 MSDC Timing Diagram (DDR50 mode)

Table 3-12 and Figure 3-7 present the MSDC timing characteristics in HS200 mode.

Table 3-12 MSDC Timing Characteristics (HS200 mode)

No	Parameter		Min	Max	Unit
Clock CLK					
HS2001	t_C	Cycle time, CLK	5		ns
HS2002	t_{RISE_CLK}	Rise time, CLK (C_{Device} ≤ 6 pF)		1	ns
HS2003	t_{FALL_CLK}	Fall time, CLK (C_{Device} ≤ 6 pF)		1	ns
	D	Duty Cycle, CLK	30	70	%
Input DAT/CMD; C_{Device} ≤ 6 pF					
HS2005	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input	1.4		ns
HS2006	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input	0.8		ns
Output DAT/CMD					
HS2007	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output	0	2	UI(1)
	$\Delta t_{d\_DAT/CMD}$	Delay variation due to temperature change after tuning(2)	-350 (ΔT=-20°C)	1550 (ΔT=90°C)	ps
HS2008	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output	0.575(3)		UI(1)

1. Unit Interval (UI) is one bit nominal time. For example, UI= 5 ns at 200 MHz.
2. Total allowable shift of output valid window ($t_{h\_DAT/CMD}$) from last system tuning procedure $\Delta t_{d\_DAT/CMD}$ is 2600 ps for ΔT from -25 °C to 125 °C during operation.
3. The minimum value is equal to 2.88 ns at 208 MHz.

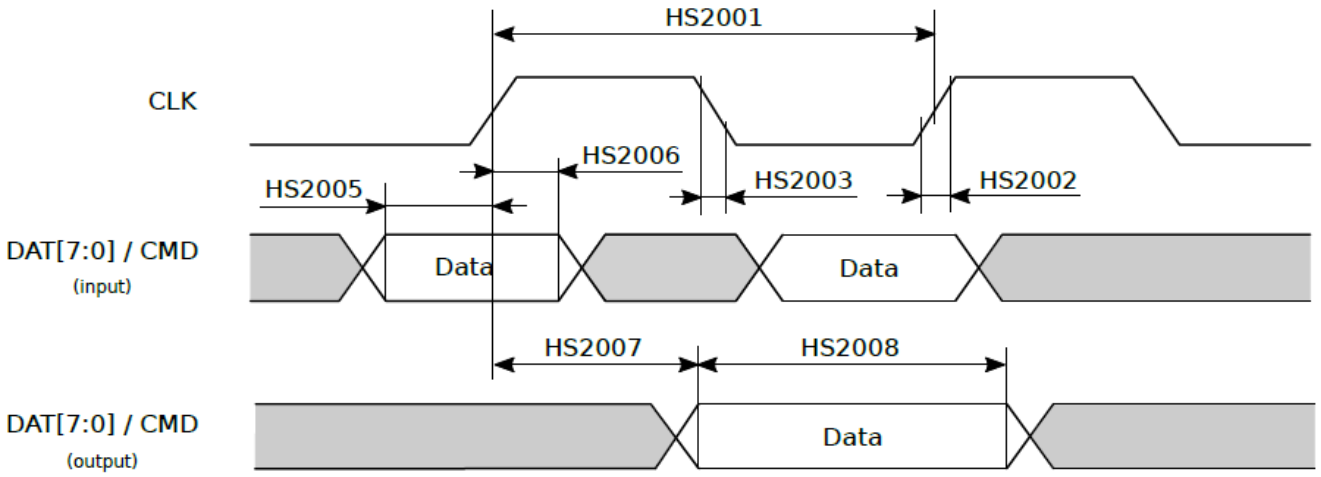


Figure 3-7 MSDC Timing Diagram (HS200 mode)

Table 3-13, Figure 3-8, and Figure 3-9 present the MSDC timing characteristics in HS400 mode.

Table 3-13 MSDC Timing Characteristics (HS400 mode)

No	Symbol	Parameter	Min	Max	Unit
Input CLK					
HS4001	t_{C_CLK}	Cycle time, CLK (with respect to V_T)	5		ns
	SR	Slew rate, with respect to V_{IH}/V_{IL}	1.125		V/ns
HS4002	t_{ck_dd}	Duty cycle distortion (1)	0	0.3	ns
HS4003	t_{W_CLK}	Pulse duration, CLK (with respect to V_T)	2.2		ns

No	Symbol	Parameter	Min	Max	Unit
Input DAT (referenced to CLK); with respect to VIH/VIL; (C_{Device} ≤ 6 pF)					
HS4004	t_{su_DAT}	Setup time, DAT input	0.4		ns
HS4005	t_{h_DAT}	Hold time, DAT input	0.4		ns
	SR	Slew rate	1.125		V/ns
Data Strobe					
HS4006	t_{C_CLK}	Cycle time, CLK (with respect to V_T)	5		ns
	SR	Slew rate (with respect to V_{OH}/V_{OL} and HS400 reference load)	1.125		V/ns
HS4007	t_{ds_dd}	Duty cycle distortion[(2)]	0	0.2	ns
HS4008	t_{W_CLK}	Pulse duration, CLK (with respect to V_T)	2		ns
	t_{RPRE}	Read pre-amble	0.4		t_{C_CLK}
	t_{RPST}	Read post-amble	0.4		t_{C_CLK}
Input DAT (referenced to Data Strobe); with respect to V_{OH}/V_{OL} and HS400 reference load					
HS4009	t_{RQ}	Output skew		0.4	ns
HS4010	t_{RQH}	Output hold skew		0.4	ns
	SR	Slew rate	1.125		V/ns

1. Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter and phase noise.
2. Allowable deviation from the input CLK duty cycle distortion (t_{ck_dd}). With respect to V_T. Includes jitter and phase noise.

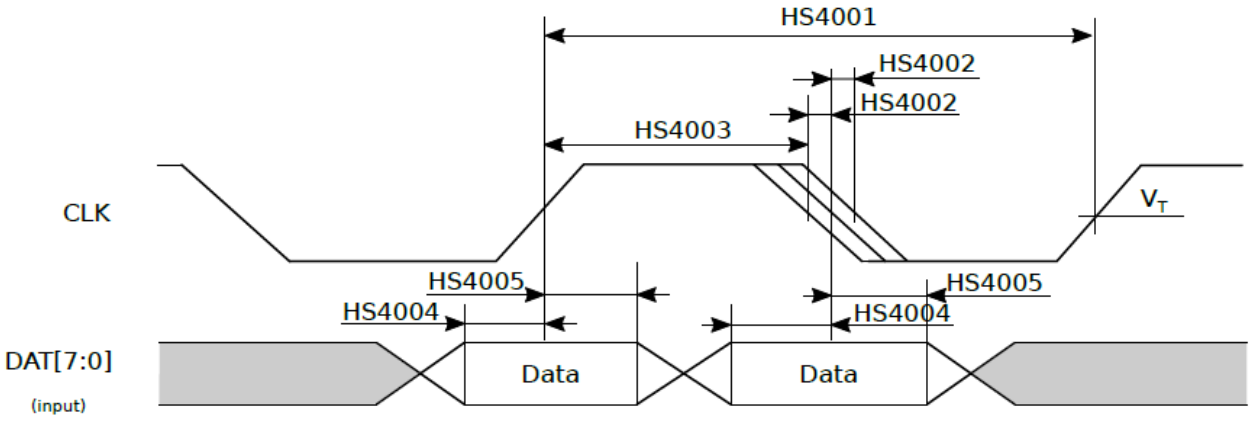


Figure 3-8 MSDC Timing Diagram (HS400 Input mode)

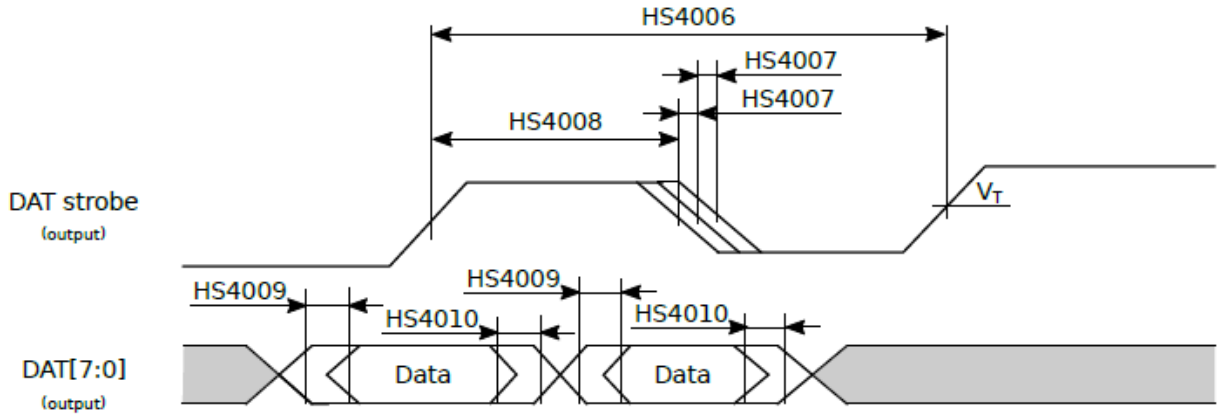


Figure 3-9 MSDC Timing Diagram (HS400 Output mode)

3.6.2 Universal Flash Storage (UFS)

The UFS controller is used for computing and mobile systems requiring low power consumption and high data throughput to store data in Non-Volatile Memory (NVM) devices. The UFS controller in the device is composed of three main modules: UFS HCI (Host Controller Interface), UniPro® and M-PHY.

The UFS controller supports the following key features:

- JEDEC Standard Universal Flash Storage Version 2.1
- JEDEC UFS HCI Version 2.1
- MIPI UniPro Version 1.6
- MIPI M-PHY Version 3.1
- One lane, up to 5.8 Gbps (HS-G3 B-series)
- AHB slave interface
- DMA AXI master interface with 36-bit address width

3.6.2.1 UFS Signal Descriptions

Table 3-14 presents UFS signal descriptions.

Table 3-14 UFS Signal Descriptions

Signal Name	Type	Description	Ball Location
UFS_MPHY_SCL	DI	UFS M-PHY serial clock	C26, L23
UFS_MPHY_SDA	DIO	UFS M-PHY serial data	G23, N27
UFS_RST_N	AIO	UFS reset	E22
UFS_RX0_RXN	AIO	UFS negative differential receive data lane 0	B22
UFS_RX0_RXP	AIO	UFS positive differential receive data lane 0	A22
UFS_TX0_N	AIO	UFS negative differential transmit data lane 0	A24
UFS_TX0_P	AIO	UFS positive differential transmit data lane 0	B24
UFS_UNIPRO_SCL	DI	UFS UniPro serial clock	C25, M24
UFS_UNIPRO_SDA	DIO	UFS UniPro serial data	B27, M25

3.7 Display

The display subsystem contains two types of data paths:

- Multimedia Data Path (MDP), which is the time-sharing data processing pipeline. The MDP includes read/write DMA engines and supports resizing and rotation operations for memory-to-memory pixel data transfers, in addition to providing 2D-sharpness enhancement, local contrast enhancement, color correction, and color enhancement functions.
- Display Data Path (DISP), which is a set of read/write DMA engines and provides overlay, color enhancement, adaptive ambient light processing, color correction, gamma correction and dither functions. The processed data can be either stored back in memory and/or delivered directly to display interface controllers like DSI, and DPI or DBI, for concurrent dual display output. The DPI port can connect to external LVDS, HDMI™, and MHL bridge chips to support these interfaces.

3.7.1 Multimedia Data Path (MDP)

The main purpose of the MDP is to generate images for display, video codec, JPEG codec and face detect.

3.7.1.1 MDP Read DMA (MDP_RDMA)

The MDP_RDMA is used to read images of multiple source formats from DRAM and output in scan line sequence to the following MDP processing engine.

The MDP_RDMA supports several functions:

- Multiple formats of input images:
  - YUV420 and YUV422 scan line 1/2/3 planes
  - RGB 16/24/32-bit
- Input image cropping/clipping
- Tile mode ready; supports source width up to 131,072 pixels
- Arbitrary byte swap for YUV or RGB source
- 3 × 3 color space conversion from RGB to YUV
- Chroma upsample to YUV444 for cosited or non-cosited YUV420 and YUV422 source data

3.7.1.2 MDP Color Correction (MDP_CCORR)

The MDP color correction engine changes the overall mixture of RGB colors to fit the characteristics of the target display panel.

The MDP_CCORR supports the following features:

- YUV to RGB, and RGB to YUV conversions
- Fixed-coefficient inverse gamma correction
- Programmable 3 × 3 conversion matrix

3.7.1.3 MDP Resizer (MDP_RSZ)

There are two resizer modules within the MDP: MDP_RSZ0 and MDP_RSZ1.

Each resizer supports the following key features:

- Three scaling algorithms (depending on the scaling ratio) including 6-tap FIR, 4n-tap cubic accumulation, and n-tap source accumulation
- 8-bit YUV444 (unsigned) input and output data format
- Scaling ratio between 1/128× and 64×
- Crop and digital zoom functions
- Maximum width of 544 pixels (tile mode)
- Edge-preserving interpolation
- Signal enhancer (pre-scaler sharpness)

3.7.1.4 MDP 2D Sharpness Engine (MDP_TDSHP)

The sharpness function provides a better picture quality for display panels by restoring the image details, sharpening the edge and delivering a vivid feeling for pictures and videos.

The MDP_TDSHP supports the following functions:

- 2-dimensional sharpness filter
- Peaking by Color (PBC)

3.7.1.5 MDP Adaptive Ambient Light Controller (MDP_AAL)

The MDP_AAL provides the following key features:

- Dark Region Enhancement (DRE) mapping for sunlight visibility
- Block-based histogram / Block-based gain-curve calculation

3.7.1.6 MDP Color Engine (COLOR)

The COLOR is a multi-stage processing engine, which is used for achieving better picture quality and making one display panel resemble another in their output characteristics. It provides color space conversion functions and various hue/luma/saturation adjustments.

The COLOR supports the following key features:

- Input/output color conversion
- Hue engine functions:
  - Partial hue: modifies hue angle of specific hue phase
- Luma engine functions:
  - Partial luma: modifies luma value of specific luma phase
  - Contrast enhancement
  - Brightness adjustment
- Saturation engine functions:
  - Partial S: modifies saturation value of specific hue phase
  - Global saturation adjustment
  - Low S protection

NOTE: The COLOR is shared with the Display Data Path (DISP).

3.7.1.7 MDP Write DMA (MDP_WDMA)

The MDP_WDMA does the job of DMA writing out the data in MDP pipeline into the DRAM.

The MDP_WDMA supports the following key features:

- Input color format: YUV444/RGB888
- Dither function
- Internal color matrix
- Byte swap, color swap, and UV swap functions
- Output formats: RGB565/RGB888/ARGB8888/UYVY/YV12/NV12/NV21

3.7.1.8 MDP Rotation DMA (MDP_WROT)

The MDP_WROT is a write rotate DMA agent, which supports 8 rotation/flip options.

The MDP_WROT provides the following key features:

- Rotation angles: 0°, 0° + H_Flip, 90°, 90° + H_Flip, 180°, 180° + H_Flip, 270°, and 270° + H_Flip
- Formats and footprints: YUV422 1/2/3 plane(s), YUV420 2/3 plane(s), RGB888, ARGB8888, RGB565, Y only
- Internal color matrix
- Dither engine

3.7.2 Display Data Path (DISP)

The DISP consists of two display pipelines. One display pipeline has its own read/write DMA engines, overlay manager, resizer, color engine, adaptive ambient light controller, color correction block, gamma correction block, and dither engine, and outputs the processed data either to a display interface controller or writes it back to memory. The other display pipeline only includes a read DMA engine and overlay manager, and outputs the data to a display interface controller.

3.7.2.1 DISP Read DMA (DISP_RDMA)

The DISP_RDMA engine reads out the data in the display pipeline from either DRAM or from upstream engines within the display pipeline, applies processing operations and delivers the data to the display interface controllers like DSI and DPI.

The DISP_RDMA supports the following key features:

- Direct link input mode
- Memory input mode
  - Input formats: YUYV422, UYVY422, YVYU422, UYVY422, RGB565, RGB888,ARGB8888
  - Input footprints: Raster-scan mode, 64 byte-aligned tile mode
  - Slow down mode
- Output control
  - Byte swap, RGB swap
  - Progressive and interlace modes
  - Non-stop output mode, if the data buffer is under-running
- Buffer control
  - Programmable request, pre-ultra, and ultra control mechanisms

3.7.2.2 DISP Write DMA (DISP_WDMA)

The DISP_WDMA writes out the data in display pipeline into the DRAM.

The DISP_WDMA provides the following key features:

- Input color format: YUV444/RGB888
- Dither function
- Internal color matrix
- Byte swap, color swap, and UV swap functions
- Output color formats: RGB565/RGB888/ARGB8888/UYVY/YV12/NV12/NV21

3.7.2.3 DISP Overlay (DISP_OVL)

The DISP_OVL manager does alpha blending of pixel data layers. The source pixel data is fetched from DRAM by a dedicated read DMA channel for each layer. The pixel data is processed depending on pixel characteristics and the display panel requirements.
There are three DISP_OVL managers within the display data path: DISP_OVL0, DISP_OVL0_2L, and DISP_OVL1_2L.

Each DISP_OVL supports the following key features:

- Layers of blending:
  - Up to 4 layers for DISP_OVL0
  - Up to 2 layers for DISP_OVL0_2L and DISP_OVL1_2L
- Input resolution:
  - Full HD+ (2400 × 1080)
- Memory source formats: RGB565/RGB888/ARGB8888/PARGB8888/XRGB/YUV422
- Swap control:
  - RGB swap and byte swap control (RGB/BGR/xARGB/xABGR/RGBxA/BGRxA)
  - UYVY swap (UYVY/VYUY/YUYV/YVYU)
- Interleaving of left and right images for 3D display in landscape and portrait modes (supported by DISP_OVL0_2L only)
- Fixed color conversion coefficients
- Source color key or destination color key

- Pixel alpha with PARGB/ARGB, and constant alpha or surface flinger alpha blending
- Flexible Region-of-Interest (ROI) system, supporting individual color depth, window size, vertical and horizontal offsets
- Vertical, horizontal, and 180-degree flip function

3.7.2.4 DISP Color Engine (COLOR)

NOTE: The COLOR is shared with the Multimedia Data Path (MDP). For information on the supported features, see Section 3.7.1.6 MDP Color Engine (COLOR).

3.7.2.5 DISP Color Correction (DISP_CCORR)

The DISP_CCORR engine changes the overall mixture of RGB colors to fit the characteristics of target display panel.

The DISP_CCORR supports the following key features:

- Fixed-coefficient inverse gamma table
- Fixed-coefficient gamma table
- Programmable 3 × 3 matrix

3.7.2.6 DISP Adaptive Ambient Light Controller (DISP_AAL)

The DSIP_AAL controller includes content adaptive and ambient light adaptive functions. It is responsible for backlight power saving and sunlight visibility improvement.

The DISP_AAL provides the following key features:

- Weighted maxRGB/Luma histogram
- Dark Region Enhancement (DRE) mapping for sunlight visibility
- Content Adaptive Backlight Control (CABC) compensation for power saving

3.7.2.7 DISP Gamma Engine (DISP_GAMMA)

The DISP_GAMMA engine provides gamma correction by changing the overall mixture of RGB colors to fit the characteristics of the display panel.

The DISP_GAMMA supports the following key features:

- 10-bit gamma table with 512 entries

3.7.2.8 DISP Dither Engine (DISP_DITHER)

The DISP_DITHER engine is used to reduce the effect of quantization errors while decreasing the RGB depth.

The DISP_DITHER supports the following key features:

- Ordered dithering: Running order dither frame phase control
- Linear Feedback Shift Register (LFSR) dithering
- Rounding

3.7.2.9 DISP Resizer (DISP_RSZ)

The DISP_RSZ is the resizer module in the display data path.

The DISP_RSZ supports the following key features:

- Input and output format: ARGB8888
- Up-scaling only

- Scaling ratio between 1× and 64×
- 4-tap FIR
- Maximum width of 736 pixels

3.7.2.10 DISP Mutex (DISP_MUTEX)

The DISP_MUTEX is used to synchronize the start trigger signal of each submodule in the display data path. This enables the composition of up to two independent real-time display paths, or multiple soft paths, which can perform multi-tasking between several software processes.

The DISP_MUTEX supports the following key features:

- Up to 12 mutex cores in parallel
- Each submodule in the display data path can be assigned to any one of the 12 mutex cores
- Start trigger signal selection for each mutex core: driven either from SW or from a display interface (DSI, DPI, DBI)

The start trigger method determines the operation mode of the display data path:

- Single mode (SW trigger):
  - Single frame processing upon every SW trigger
  - Memory in—memory out path (not always being single mode)
  - Memory in and direct link to command mode display output (for example, DSI command mode)
- Refresh mode (display interface trigger):
  - Frame-by-frame processing after start
  - Memory in and direct link to video mode display output (for example, DSI video mode, DPI)

3.7.3 Display Parallel Interface (DPI)

The DPI controller provides data to companion chips, such as HDMI, MHL, or other bridge chips.

The DPI controller supports the following key features:

- Resolution up to 1920p × 1080p @ 30fps
- Programmable 2D/3D, progressive/interlaced timing generator
- Programmable EAV and SAV embedded synchronization timing
- Fixed-coefficient color space transformation
- RGB888/YUV444 8-bit/YUV422 8-bit, 10-bit, 12-bit output dataformats
- YC MUX (CCIR656-like) output format
- Dual edge output format
- Secure display
- 3-tap chroma Low-Pass Filter (LPF)
- Internal pattern generator

3.7.3.1 DPI Signal Descriptions

Table 3-15 presents DPI signal descriptions.

Table 3-15 DPI Signal Descriptions

Signal Name	Type	Description	Ball Location
DBPI_CK	DO	Display pixel clock	AC25
DBPI_D0	DIO	Display pixel data 0	W23
DBPI_D1	DIO	Display pixel data 1	AA25

Signal Name	Type	Description	Ball Location
DBPI_D2	DIO	Display pixel data 2	W25
DBPI_D3	DIO	Display pixel data 3	W26
DBPI_D4	DIO	Display pixel data 4	AB26
DBPI_D5	DIO	Display pixel data 5	AB23
DBPI_D6	DIO	Display pixel data 6	W24
DBPI_D7	DIO	Display pixel data 7	Y24
DBPI_D8	DIO	Display pixel data 8	AB24
DBPI_D9	DIO	Display pixel data 9	Y26
DBPI_D10	DIO	Display pixel data 10	AA26
DBPI_D11	DIO	Display pixel data 11	AA23
DBPI_DE	DO	Display pixel data enable	AC26
DBPI_HSYNC	DO	Display horizontal sync	Y23
DBPI_VSYNC	DO	Display vertical sync	AA24

NOTE: The DPI shares pins with DBI (see Section 3.7.4.1 DBI Signal Descriptions) and the two interfaces cannot be used concurrently.

Table 3-16 presents the DPI pixel data signals mapping for four data/clock timing combinations in dual edge mode. In dual edge mode, one pixel is sent by two pixel clock edges.

Table 3-16 DPI Signals Mapping in Dual Edge Mode

Signal Name	Case 1		Case 2		Case 3		Case 4	
	Rising edge	Falling edge	Rising edge	Falling edge	Falling edge	Rising edge	Falling edge	Rising edge
DBPI_D0	G4	B0	B0	G4	G4	B0	B0	G4
DBPI_D1	G5	B1	B1	G5	G5	B1	B1	G5
DBPI_D2	G6	B2	B2	G6	G6	B2	B2	G6
DBPI_D3	G7	B3	B3	G7	G7	B3	B3	G7
DBPI_D4	R0	B4	B4	R0	R0	B4	B4	R0
DBPI_D5	R1	B5	B5	R1	R1	B5	B5	R1
DBPI_D6	R2	B6	B6	R2	R2	B6	B6	R2
DBPI_D7	R3	B7	B7	R3	R3	B7	B7	R3
DBPI_D8	R4	G0	G0	R4	R4	G0	G0	R4
DBPI_D9	R5	G1	G1	R5	R5	G1	G1	R5
DBPI_D10	R6	G2	G2	R6	R6	G2	G2	R6
DBPI_D11	R7	G3	G3	R7	R7	G3	G3	R7

3.7.3.2 DPI Timing Characteristics

Table 3-17 and Figure 3-10 present timing characteristics for DPI in the device.

Table 3-17 DPI Timing Characteristics

No.	Parameter		Min	Max	Unit
DPI01	t_c	Cycle time	13.47(1)		ns
DPI02	D	Duty cycle, DPI_CK	45	55	%
DPI03	t_{RISE}	Rise time		2.69	ns
DPI04	t_{FALL}	Fall time		2.69	ns

No.	Parameter		Min	Max	Unit
DPI05	t_d	Delay time, other signals to DBPI_CK	3.69		ns

1. For maximum operating clock frequency refer to Table 6-1.

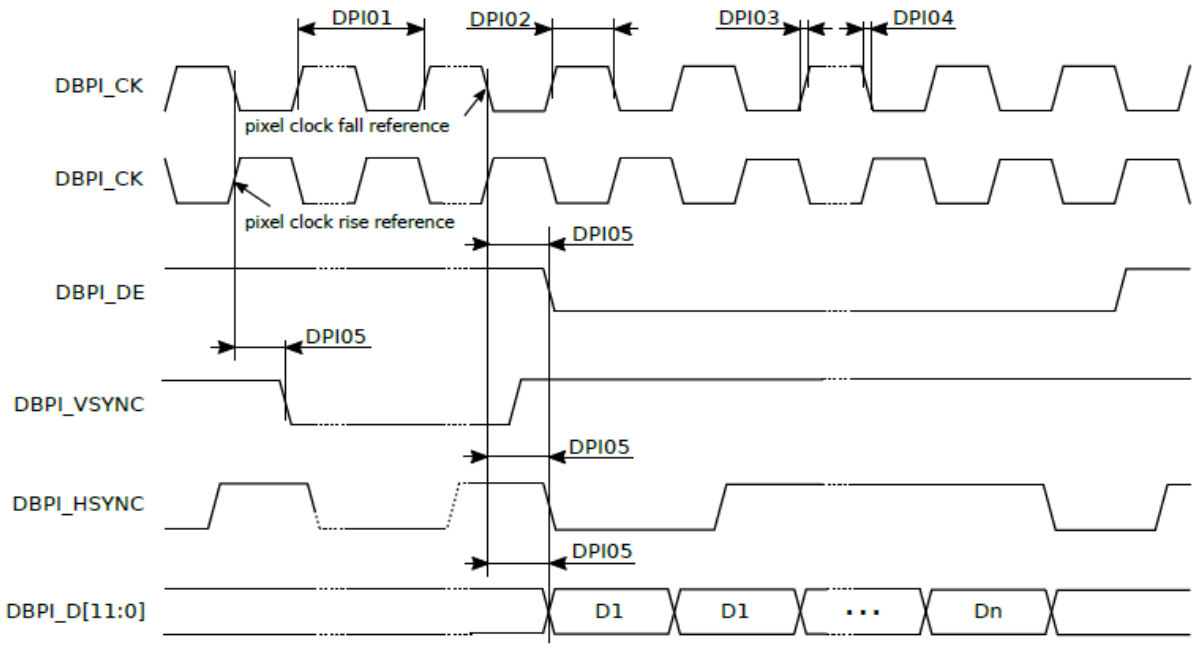


Figure 3-10 DPI Timing Diagram

3.7.4 Display Bus Interface (DBI)

The DBI controller provides data in MIPI DBI-B or DBI-C format to a mobile Liquid Crystal Monitor (LCM).

The DBI controller provides the following key features:

- DBI Type B support:
  - 8-bit or 9-bit parallel interface
  - RGB666 color format
  - Resolution up to 320 × 480 @ 30fps
- DBI Type C support:
  - 9-bit (Option 1) or 8-bit (Option 3) serial interface
  - RGB666 color format
  - Resolution up to 240 × 240 @ 30fps for 1 data lane
  - Resolution up to 400 × 400 @ 30fps for 2 data lanes
- Tearing Effect (TE) synchronization
- Embedded dither processor, which can be used to keep the picture quality during bit drop of each color channel
  - Separate/independent dithering depth for each color channel
  - Four dithering modes:
    - Rounding
    - Randomize
    - Error diffusion
    - Running order dithering

3.7.4.1 DBI Signal Descriptions

Table 3-18 presents DBI signal descriptions.

Table 3-18 DBI Signal Descriptions

Signal Name	Type	Description	Ball Location
DBI Type B			
DBPI_CK	DO	Chip select	AC25
DBPI_D0	DIO	Display command or pixel data 0	W23
DBPI_D1	DIO	Display command or pixel data 1	AA25
DBPI_D2	DIO	Display command or pixel data 2	W25
DBPI_D3	DIO	Display command or pixel data 3	W26
DBPI_D4	DIO	Display command or pixel data 4	AB26
DBPI_D5	DIO	Display command or pixel data 5	AB23
DBPI_D6	DIO	Display command or pixel data 6	W24
DBPI_D7	DIO	Display command or pixel data 7	Y24
DBPI_D8	DIO	Display command or pixel data 8	AB24
DBPI_DE	DO	Command/data select	AC26
DBPI_HSYNC	DO	Write strobe	Y23
DBPI_VSYNC	DO	Read strobe	AA24
DBI Type C			
DBPI_CK	DO	Synchronous clock	AC25
DBPI_D11	DIO	Serial data input/output	AA23
DBPI_DE	DO	Command/data select	AC26
DBPI_HSYNC	DO	Chip select	Y23

NOTE: The DBI shares pins with DPI (see Section 3.7.3.1 DPI Signal Descriptions) and the two interfaces cannot be used concurrently.

3.7.5 Display Serial Interface (DSI)

The DSI is based on MIPI Alliance Specification, supporting high-speed serial data transfer between host processor and peripheral devices such as display modules.

The DSI module receives frame pixels from memory, performs frames packing and lane distribution, and then sends the data to the MIPI D-PHY TX core for serializing.

The DSI module has the following key features for display serial interface:

- Supports video and command mode data transfers
- 1 clock lane and up to 4 data lanes
- Throughput up to 1.5 Gbps per data lane
- Resolution up to 2400 × 1080 @ 60fps
- Bi-directional data transmission in Low-Power mode in data lane 0
- Uni-directional data transmission in High-Speed mode in data lanes 0 through 3
- Non-continuous high-speed transmission in clock and data lanes
- Pixel formats supported: RGB565 / RGB666 / loosely RGB666 / RGB888
- 128-entry command queue for command transmission
- 3 types of video modes: sync-event, sync-pulse, and burst modes

- Limited high-speed residual packet transmission during video mode blanking period
- Ultra-low power mode control
- Peripheral and external Tearing Effect (TE) signals detection
- Command mode frame transmission free-run
- Low Frame-Rate (LFR) technique

3.7.5.1 DSI Signal Descriptions

Table 3-19 presents DSI signal descriptions.

Table 3-19 DSI Signal Descriptions

Signal Name	Type	Description	Ball Location
DSI0_CKN	AIO	DSI0 clock lane N	U24
DSI0_CKP	AIO	DSI0 clock lane P	U25
DSI0_D0N	AIO	DSI0 data lane0 N	R27
DSI0_D0P	AIO	DSI0 data lane0 P	T27
DSI0_D1N	AIO	DSI0 data lane1 N	T26
DSI0_D1P	AIO	DSI0 data lane1 P	U26
DSI0_D2N	AIO	DSI0 data lane2 N	V24
DSI0_D2P	AIO	DSI0 data lane2 P	V25
DSI0_D3N	AIO	DSI0 data lane3 N	T24
DSI0_D3P	AIO	DSI0 data lane3 P	T25
DSI_TE	DI	DSI tearing effect control	AG26

3.7.5.2 DSI Timing Characteristics

The DSI interface timing and electrical characteristics are compliant with MIPI DSI Specification v01-02-00 and MIPI D-PHY Specification v1-1.

3.7.6 Display Pulse Width Modulation (DISP PWM) and Reset

The DISP PWM module provides a PWM signal for the LED driver of an LCM in order to reduce its backlight power consumption.

The DISP PWM supports the following features:

- Gradual PWM control
- Operating clock: 26 MHz, 104 MHz, 16 MHz, 63 MHz or 125 MHz

Additionally, the device provides the LCM_RST signal that can be used to reset an external LCM.

Table 3-20 presents the DISP PWM and reset signal descriptions.

Table 3-20 DISP PWM and Reset Signal Descriptions

Signal Name	Type	Description	Ball Location
DISP_PWM	DO	Display PWM output	AH23
LCM_RST	DO	Display reset	AH27

3.8 Imaging

The imaging subsystem is built around a feature-rich Image Signal Processor (ISP), which processes either data received from camera sensors through MIPI CSI-2 interface or RAW data fetched from DRAM, and an ancillary engine for face detection and visual tracking.

3.8.1 Camera Image Signal Processor (ISP)

The ISP consists of timing generation unit, a lens and sensor compensation unit, and an image processing unit. The ISP works on image data received either from one of the camera interfaces or from system DRAM, and outputs the processed data back into DRAM.

Figure 3-11 shows the ISP internal block diagram.

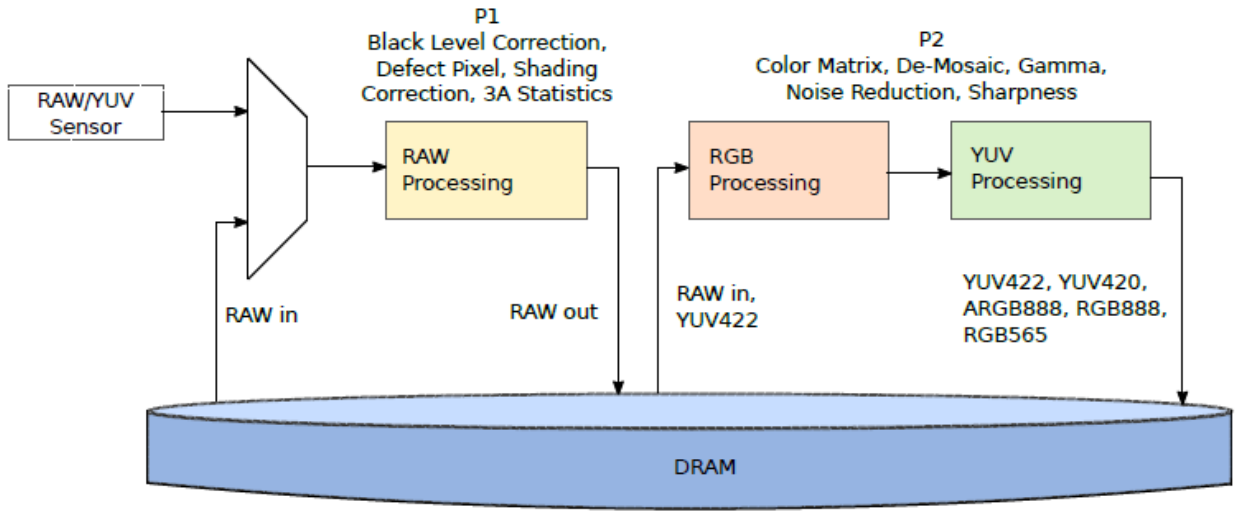


Figure 3-11 Image Signal Processor Block Diagram

The following list highlights the ISP features:

- Camera interfaces:
  - Primary camera: MIPI CSI-2 with 4 data lanes
  - Secondary camera: MIPI CSI-2 with 4 data lanes
  - Tertiary camera: MIPI CSI-2 with 4 data lanes
- 32MP @ 30fps processing
- PIP (picture in picture), (16MP + 16MP) @ 30fps
- Lens and sensor compensation and image processing units:
  - Defective pixel compensation
  - Lens shading compensation
  - De-mosaic
  - Color clipping
  - Gamma correction
  - Edge enhancement (sharpness)
  - Noise reduction with large kernel
    - Multi-frame noise reduction for image capture
    - Temporal noise reduction for video recording
  - Preference color adaptation
  - 3A (AE/AWB/AF) statistics and correction

- Hardware JPEG encoder:
  - Baseline encoding with 200MP/sec
  - Continuous shotwith 25MP @ 7fps
- Supports YUV422/YUV420 color format and EXIF/JFIF format
- Video face beautification
- Flicker detection
- Electronic image stabilization, and digital image stabilization for video
- High quality resizer engines with 90° and 180° image rotation

3.8.1.1 Camera Signal Descriptions

Table 3-21 presents CAM signal descriptions.

Table 3-21 CAM Signal Descriptions

Signal Name	Type	Description	Ball Location
CMFLASH	DO	Camera flash strobe	AE2, R25, M22
CMMCLK0	DO	Sensor reference clock 0	AA4
CMMCLK1	DO	Sensor reference clock 1	AC2
CMMCLK2	DO	Sensor reference clock 2	W4, AA6, AE3, K4, Y22, Y25
CMMCLK3	DO	Sensor reference clock 3	Y4, AH1, L4, AA22, AD25
CMVREF0	DO	Camera Frame Sync	W5, L25, L22
CMVREF1	DO	Camera Frame Sync	AA3, P22, AD25

3.8.2 Face Detection and Visual Tracking (FDVT)

The Face Detection and Visual Tracking (FDVT) engine is used to detect the new coming faces and track the existing faces in an image. The input image of the FDVT is the 16-bit RGB565 data generated by the ISP module.

The FDVT supports the following key features:

- Detecting faces of Rotation-in-Plane (RIP) from -180° to +180°
- Detecting faces of Rotation-off-Plane (ROP) from -90° to +90°
- Maximum image size of 320 x 240 pixels

3.8.3 Camera Serial Interface (CSI)

The device features three MIPI CSI-2 modules that are fully compliant with MIPI CSI-2 specification. The primary CSI-2 interface (CSI0) uses a combined MIPI D-PHY/C-PHY layer, while the secondary (CSI1) and tertiary (CSI2) interfaces implement only a MIPI D-PHY layers. The PHY layer of each interface acts as a physical link between the CSI controllers and the image sensors.

The D-PHY layer primarily feeds in the CSI data and clock lanes. The D-PHY layer provides high-speed clock, which can achieve up to 1.5 Gbps throughput, as a primary clock to the CSI controller. Half-speed, 768-MHz clock is also supported.

The MIPI CSI-2 implementation in the device provides the following key features:

- Primary CSI-2 interface (CSI0), which can be used in one of the following three configurations:
  - One 4-data lane interface in D-PHY mode

  - Two 2-data lane interfaces in D-PHY mode
  - 3-trio interfaces in C-PHY mode
- Secondary CSI-2 interface (CSI1), configured with 4-data lanes in D-PHY mode
- Tertiary CSI-2 interface (CSI2), configured with 4-data lanes in D-PHY mode
- D-PHY throughput up to 2.8 Gbps for one datalane
- C-PHY throughput up to 2.5 Gbps for one datalane
- Pixel format of 10-bit RAW8/RAW10/RAW12/RAW14/YUV422
- Four virtual channels

3.8.3.1 CSI Signal Descriptions

Table 3-22 presents CSI0 signal descriptions.

Table 3-22 CSI0 Signal Descriptions

Signal Name	Type	Description			Ball Location
		4-lane D-PHY Mode	2 x 2-lane D-PHY Mode	3-trio C-PHY Mode	
CSI0A_L0P_T0A	AO	CSI0 data lane 2, positive	CSI0_A data lane 0, positive	CSI0 Trio0 A	P4
CSI0A_L0N_T0B	AIO	CSI0 data lane 2, negative	CSI0_A data lane 0, negative	CSI0 Trio0 B	P3
CSI0A_L1P_T0C	AIO	CSI0 data lane 0, positive	CSI0_A clock lane, positive	CSI0 Trio0 C	R2
CSI0A_L1N_T1A	AIO	CSI0 data lane 0, negative	CSI0_A clock lane, negative	CSI0 Trio1 A	R1
CSI0A_L2P_T1B	AIO	CSI0 clock lane, positive	CSI0_A data lane 1, positive	CSI0 Trio1 B	P5
CSI0A_L2N_T1C	AIO	CSI0 clock lane, negative	CSI0_A data lane 1, negative	CSI0 Trio1 C	N5
CSI0B_L0P_T0A	AIO	CSI0 data lane 1, positive	CSI0_B data lane 0, positive	CSI0 Trio2 A	R3
CSI0B_L0N_T0B	AIO	CSI0 data lane 1, negative	CSI0_B data lane 0, negative	CSI0 Trio2 B	R4
CSI0B_L1P_T0C	AIO	CSI0 data lane 3, positive	CSI0_B clock lane, positive	CSI0 Trio2 C	T2
CSI0B_L1N_T1A	AIO	CSI0 data lane 3, negative	CSI0_B clock lane, negative	-	T1
CSI0B_L2P_T1B	AIO	-	CSI0_B data lane 1, positive	-	T3
CSI0B_L2N_T1C	AIO	-	CSI0_B data lane 1, negative	-	T4

Table 3-23 presents CSI1 and CSI2 signal descriptions.

Table 3-23 CSI1 and CSI2 Signal Descriptions

Signal Name	Type	Description	Ball Location
MIPI CSI1 (4-lane D-PHY Mode)			

Signal Name	Type	Description	Ball Location
CSI1A_L0N	AIO	CSI1 data lane 2, negative	M1
CSI1A_L0P	AIO	CSI1 data lane 2, positive	M2
CSI1A_L1N	AIO	CSI1 data lane 0, negative	M4
CSI1A_L1P	AIO	CSI1 data lane 0, positive	M3
CSI1A_L2N	AIO	CSI1 clock lane, negative	N2
CSI1A_L2P	AIO	CSI1 clock lane, positive	N1
CSI1B_L0N	AIO	CSI1 data lane 1, negative	N4
CSI1B_L0P	AIO	CSI1 data lane 1, positive	N3
CSI1B_L1N	AIO	CSI1 data lane 3, negative	P1
CSI1B_L1P	AIO	CSI1 data lane 3, positive	P2
MIPI CSI2 (4-lane D-PHY Mode)			
CSI2A_L0N	AIO	CSI2 data lane 2, negative	U1
CSI2A_L0P	AIO	CSI2 data lane 2, positive	U2
CSI2A_L1N	AIO	CSI2 data lane 0, negative	R5
CSI2A_L1P	AIO	CSI2 data lane 0, positive	T5
CSI2A_L2N	AIO	CSI2 clock lane, negative	U3
CSI2A_L2P	AIO	CSI2 clock lane, positive	U4
CSI2B_L0N	AIO	CSI2 data lane 1, negative	V1
CSI2B_L0P	AIO	CSI2 data lane 1, positive	V2
CSI2B_L1N	AIO	CSI2 data lane 3, negative	V3
CSI2B_L1P	AIO	CSI2 data lane 3, positive	V4

3.8.3.2 CSI Timing Characteristics

Table 3-24 presents timing characteristics for CSI in the device for D-PHY mode.

Table 3-24 CSI Timing Characteristics for D-PHY Mode

Parameter		Min	Typ	Max	Unit
LP Mode					
V_{OH}	Output voltage high	1.1	1.2	1.3	V
V_{OL}	Output voltage low	-0.05		0.05	V
HS Mode					
V_{OH}	Output high voltage for non-transition bit			0.36	V
V_{OD_PP}	Transmit differential voltage	0.14	0.2	0.27	V
Clock					
t_{RISE}	Rise time			0.3	UI(1)
t_{FALL}	Fall time			0.3	UI(1)
Data					
t_{RISE}	Rise time			0.3	UI(1)
t_{FALL}	Fall time			0.3	UI(1)
Skew					
Data_Clock	Clock to data output skew	-0.15		0.15	UI(1)

1. UI = Unit Interval

3.9 Video

There are 2 video accelerators in the device—the Video Encoder (VENC) and the Video Decoder (VDEC).

3.9.1 Video Encoder (VENC)

The VENC accelerator supports main stream H.264 video encoding. It is capable of encoding 1080p video at 30fps with superior quality video quality. The VENC supports various encoding methods that satisfy basic requirements of easy software controllability. The VENC brings astonishing high quality and low memory bandwidth requirements, with advanced encoding technology. The accelerator also considers the usage of portable devices and provides several power saving capabilities.

The VENC has the following main features:

- Uses DRAM as an input, output, and working buffer
- Reads input frame buffers, executes video encoding and writes encoded bitstream to the output buffer
- Support of H.264 encoding format
- Support of YUV420 two plane scan line (NV12/NV21) and YUV420 three plane scan line (YV12/I420) color formats

Table 3-25 shows the supported video formats and their capabilities.

Table 3-25 VENC Supported Formats

Format	Feature	Details
H.264 Encoding	Profile	High
	Level	4.1
	Speed	1080p @ 30fps

3.9.2 Video Decoder (VDEC)

The VDEC accelerator provides multi-standard video decoding feature. The main purpose of the accelerator is to relieve CPU usage while providing high performance video decompression. The input to VDEC is a compressed video bitstream. After the decoding process, the reconstructed video is written into DRAM and then sent to the display subsystem.

The VDEC supports various multimedia video formats, including:

- HEVC decoder:
  - Main profile 1080p @ 30fps (40 Mbps)
- H.264 decoder:
  - Constrained Baseline profile 1080p @ 30fps (40 Mbps)
  - Main/High profile 1080p @ 30fps (40 Mbps)
- MPEG-4 decoder:
  - SP/ASP 1080p @ 30fps (40 Mbps)
- H.263 1080p @ 30fps (40 Mbps)
- DIVX3/DIVX4/DIVX5/DIVX6/DIVX HD/XVID
- MPEG-1
- MPEG-2 decoder:
  - 1080p @ 30fps (40 Mbps)
- Adaptive MPEG de-blocking filter for MPEG-2 and H.263

The VDEC supports Full HD at 30fps under the limitation of picture size > Full HD (it does not support picture width > 1920p or picture height > 1088p).

3.10 Audio

The device includes one audio subsystem providing audio data exchange features.

The audio subsystem includes the following key components:

- 1 × Slave I²S™ input interface with FM radio Sampling Rate Converter (SRC)
- 3 × Master I²S outputs
- 2 × Master I²S inputs
- 1 × Master TDM 8-channel output for MHL
- Proprietary audio interface for MTK PMIC CODEC
- PCM/I2S merged interface for MTK connectivity IC
- PCM interface for external MODEM
- 1 × PDM interface for DMIC
- Audio Front-End (AFE)

Figure 3-12 shows the Audio interfaces block diagram.

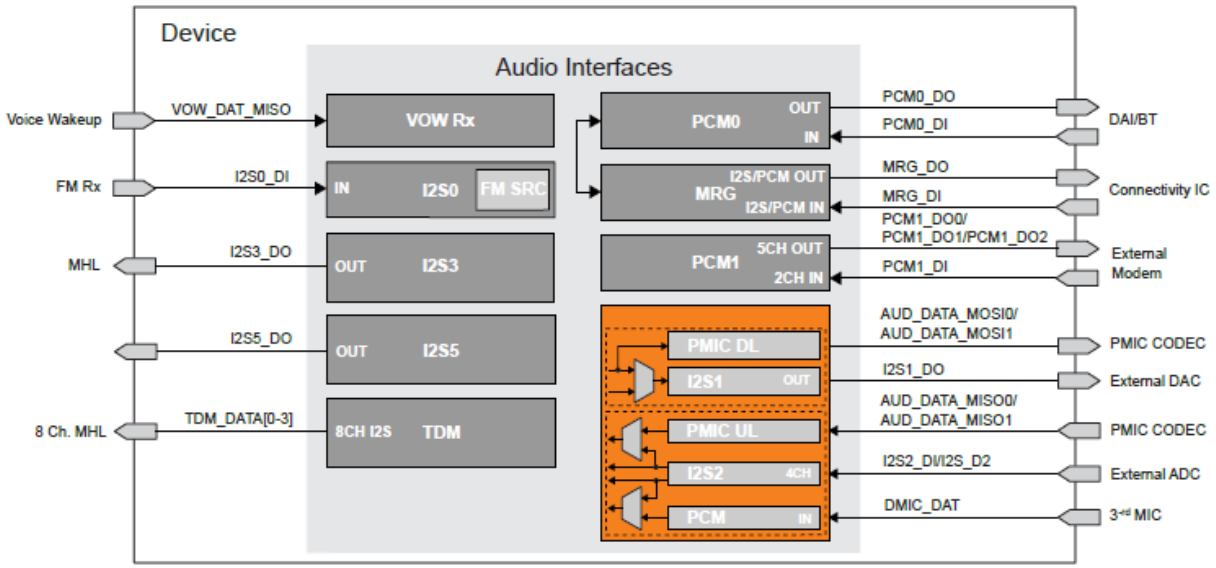


Figure 3-12 Audio Interfaces Block Diagram

3.10.1 Inter-IC Sound (I2S)

The device includes five standalone I2S modules with the following key features:

- I2S0 supports master and slave input modes with FM SRC
- I2S1, I2S3, and I2S5 support master output mode
- I2S2 supports master input mode and 2 stereo channels
- Support of 16- and 24-bit stereo data
- Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz sampling rates
- Support of EIAJ and I²S protocol formats

3.10.1.1 I2S Signal Descriptions

Table 3-26 presents I2S signal descriptions.

Table 3-26 I2S Signal Descriptions

Signal Name	Type	Description	Ball Location
I2S0			
I2S0_BCK	DIO	I2S0 serial bit clock	AF2, AA25, M26
I2S0_DI	DI	I2S0 serial data input	AE1, W26, L23, AG19
I2S0_LRCK	DIO	I2S0 word select (left/right audio channel)	AE2, W25, N24
I2S0_MCK	DO	I2S0 master clock	AC3, W23, M25
I2S1			
I2S1_BCK	DO	I2S1 serial bit clock	AA24, AJ2, L26, AG23
I2S1_DO	DO	I2S1 serial data output	AC25, AH2, N27, AG21
I2S1_LRCK	DO	I2S1 word select (left/right audio channel)	AC26, AG3, J22, AD21
I2S1_MCK	DO	I2S1 master clock	Y23, AF3, M24, AD20
I2S2			
I2S2_BCK	DO	I2S2 serial bit clock	Y26, Y5
I2S2_DI	DI	I2S2 serial data input	AA23, AA2, AG19
I2S2_DI2	DI	I2S2 serial data input	P26, AE3, AG19
I2S2_LRCK	DO	I2S2 word select (left/right audio channel)	AA26, AA3
I2S2_MCK	DO	I2S2 master clock	AB24, W6
I2S3			
I2S3_BCK	DO	I2S3 serial bit clock	AB4, AB23, AG23
I2S3_DO	DO	I2S3 serial data output	AG1, Y24, AG21
I2S3_LRCK	DO	I2S3 word select (left/right audio channel)	AG2, W24, AD21
I2S3_MCK	DO	I2S3 master clock	AB5, AB26, AD20
I2S5			
I2S5_BCK	DO	I2S5 serial bit clock	P26, W5, AG23
I2S5_DO	DO	I2S5 serial data output	AG24, AH1, AG21
I2S5_LRCK	DO	I2S5 word select (left/right audio channel)	AG25, AA6, AD21
I2S5_MCK	DO	I2S5 master clock	N26, AE3, AD20

3.10.1.2 I2S Timing Characteristics

Table 3-27 and Figure 3-13 present timing characteristics for I2S modules in the device.

Table 3-27 I2S Timing Characteristics

No.	Parameter	Description	Min	Typ	Max	Unit
-	f_S	Sampling frequency	8		192	kHz
IIS01	f_{c_MCK}	Cycle time, MCK (master clock)			24.576	MHz
-	f_{OP_BCK}	Operation frequency, BCK	$32 \times f_S$		$64 \times f_S$	MHz
IIS03	t_{c_BCK}	Cycle time, BCK	81		3906	ns
IIS04	$t_{w\_BCK\_H}$	Pulse duration, BCK high		0.5		$1 / t_{c\_BCK}$
IIS05	$t_{w\_BCK\_L}$	Pulse duration, BCK low		0.5		$1 / t_{c\_BCK}$
-	t_{LRCK}	LRCK period	32		64	$1 / t_{c\_BCK}$
IIS06	t_{v_LRCK}	BCK negative edge to LRCK valid			0.2	$1 / t_{c\_BCK}$
IIS07	t_{v_DO}	BCK negative edge to DO valid			0.2	$1 / t_{c\_BCK}$
IIS08	t_{su}	Setup time, DI	0.2			$1 / t_{c\_BCK}$
IIS10	t_h	Hold time, DI	0.2			$1 / t_{c\_BCK}$

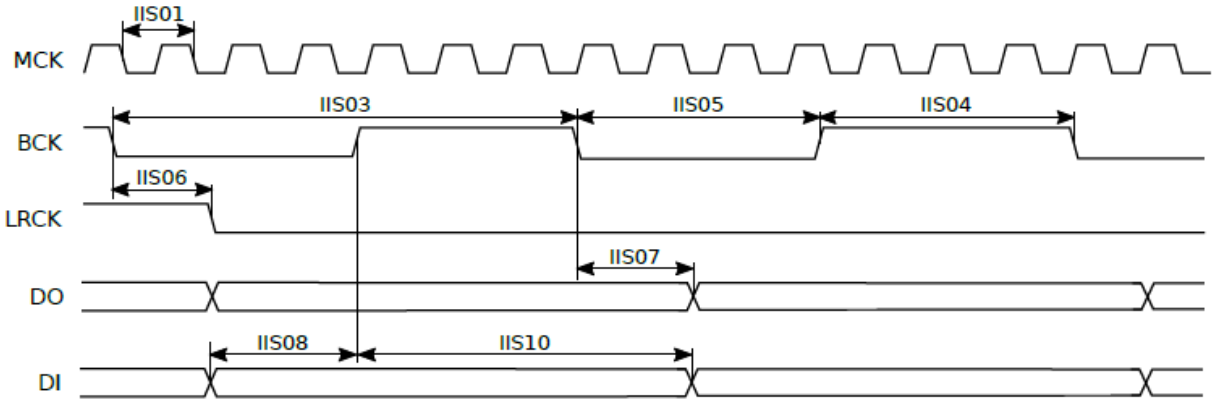


Figure 3-13 I2S Timing Diagram

3.10.2 Pulse Code Modulation (PCM)

The device includes two PCM interfaces with the following key features:

- 4-pin merged interface for concurrently supporting I2S and PCM
- PCM supports 8 and 16 kHz sampling rates
- I2S supports 32, 44.1, and 48 kHz sampling rates

3.10.2.1 PCM Signal Descriptions

Table 3-28 presents PCM signal descriptions.

Table 3-28 PCM Signal Descriptions

Signal Name	Type	Description	Ball Location
PCM0			
PCM0_CLK	DO	PCM0 clock	AB4, AA25
PCM0_DI	DI	PCM0 data input	AG1, W26
PCM0_DO	DO	PCM0 data output	AG2, W25
PCM0_SYNC	DO	PCM0 sync	AB5, W23
PCM1			
PCM1_CLK	DIO	PCM1 clock	AC24
PCM1_DI	DI	PCM1 data input	AD27
PCM1_DO0	DO	PCM1 data output 0	AD24
PCM1_DO1	DO	PCM1 data output 1	AE26
PCM1_DO2	DO	PCM1 data output 2	AC23
PCM1_SYNC	DIO	PCM1 sync	AD26

3.10.2.2 PCM Timing Characteristics

Table 3-29, Figure 3-14 and Figure 3-15 present timing characteristics for PCM interface in the device.

Table 3-29 PCM Timing Characteristics

No.	Parameter	Description	Min	Typ	Max	Unit
-	f_S	Sampling frequency	8		48	KHz
PCM1	f_{CLK}	Serial clock frequency	32 × f_S		64 × f_S	MHz
-	t_{SYNC}	Sync period	32		64	1 / f_{BCK}
PCM2	$t_{w\_CLK\_H}$	Pulse duration, CLK high		0.5		1 / f_{BCK}

No.	Parameter	Description	Min	Typ	Max	Unit
PCM3	$t_{w\_CLK\_L}$	Pulse duration, CLK low		0.5		1 / f_{BCK}
PCM4	$t_{d\_CLK\_SYNC}$	Delay time, output CLK low to SYNC valid			65	ns
PCM5	$t_{d\_CLK\_TX}$	Delay time, output CLK low to TX valid			65	ns
PCM6	t_{su}	Setup time, RX master mode	65			ns
PCM7	t_h	Hold time, RX master mode	65			ns
PCM8	t_{su}	Setup time, RX slave mode	65			ns
PCM9	t_h	Hold time, RX slave mode	65			ns

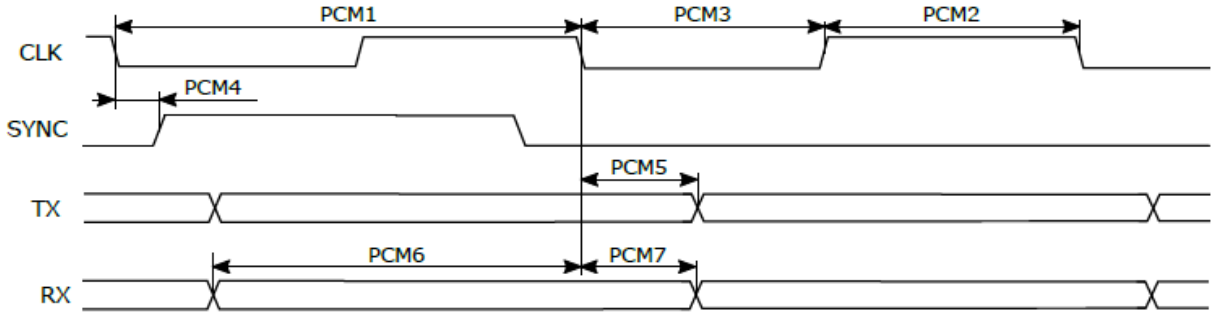


Figure 3-14 PCM Master Mode Timing Diagram

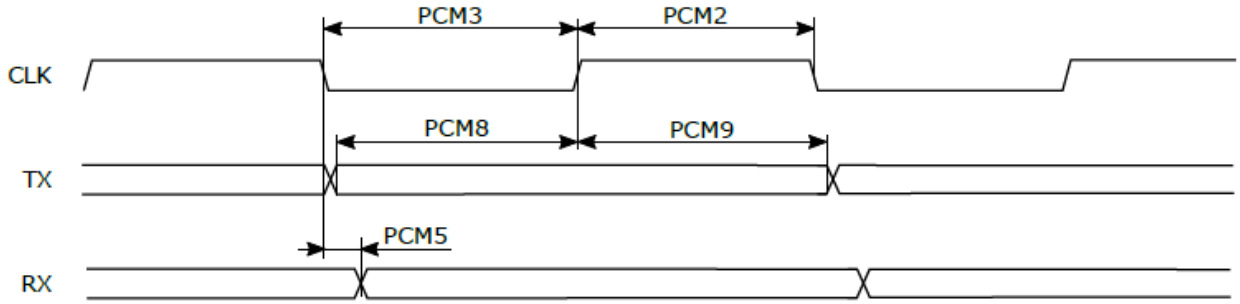


Figure 3-15 PCM Slave Mode Timing Diagram

3.10.3 Time Division Multiplexed (TDM)

The TDM Interface is a digital multiplexing technique for combining several low-rate digital channels into one high-rate channel. The device features one TDM TX interface with independent clock signals.

The TDM TX includes the following key features:

- TDM I2S output (master mode only)
- 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, and 192 kHz sampling rates
- 2, 4, or 8 audio channels in 1, 2, or 4 data pins correspondingly
- Dedicated pins for TDM TX

3.10.3.1 TDM Signal Descriptions

Table 3-30 presents TDM signal descriptions.

Table 3-30 TDM Signal Descriptions

Signal Name	Type	Description	Ball Location
TDM_BCK	DO	TDM clock (channel 1)	AC3
TDM_BCK_2nd	DO	TDM clock (channel 2)	AD25
TDM_DATA0	DO	TDM data0 output (channel 1)	AE2
TDM_DATA0_2nd	DO	TDM data0 output (channel 2)	AD21
TDM_DATA1	DO	TDM data1 output (channel 1)	AE1
TDM_DATA1_2nd	DO	TDM data1 output (channel 2)	AG21
TDM_DATA2	DO	TDM data2 output (channel 1)	AD4
TDM_DATA2_2nd	DO	TDM data2 output (channel 2)	AD20
TDM_DATA3	DO	TDM data3 output (channel 1)	Y4
TDM_DATA3_2nd	DO	TDM data3 output (channel 2)	AG19
TDM_LRCK	DO	TDM LRCK (channel 1)	AF2
TDM_LRCK_2nd	DO	TDM LRCK (channel 2)	AG23
TDM_MCK	DO	TDM master clock (channel 1)	AG1
TDM_MCK_2nd	DO	TDM master clock (channel 2)	Y25

3.10.3.2 TDM Timing Characteristics

Table 3-31 and Figure 3-16 present timing characteristics for TDM in the device.

Table 3-31 TDM Timing Characteristics

No.	Parameter	Description	Min	Typ	Max	Unit
-	f_S	Sampling frequency	8		192	KHz
TDM1	f_{MCK}	Master clock frequency	0.768		49.152	MHz
TDM2	f_{BCK}	Serial clock frequency	$32 \times f_S$		$256 \times f_S$	MHz
TDM3	$t_{w\_BCK\_H}$	Pulse duration, BCK high		0.5		$1 / f_{BCK}$
TDM4	$t_{w\_BCK\_L}$	Pulse duration, BCK low		0.5		$1 / f_{BCK}$
TDM5	t_{v_WS}	BCK negative edge to WS valid			8	ns
TDM6	t_{v_SDOUT}	BCK negative edge to SDOUT valid			8	ns
TDM7	t_{su_DI}	Setup time, DI	8			ns
TDM8	t_{h_DI}	Hold time, DI	8			ns

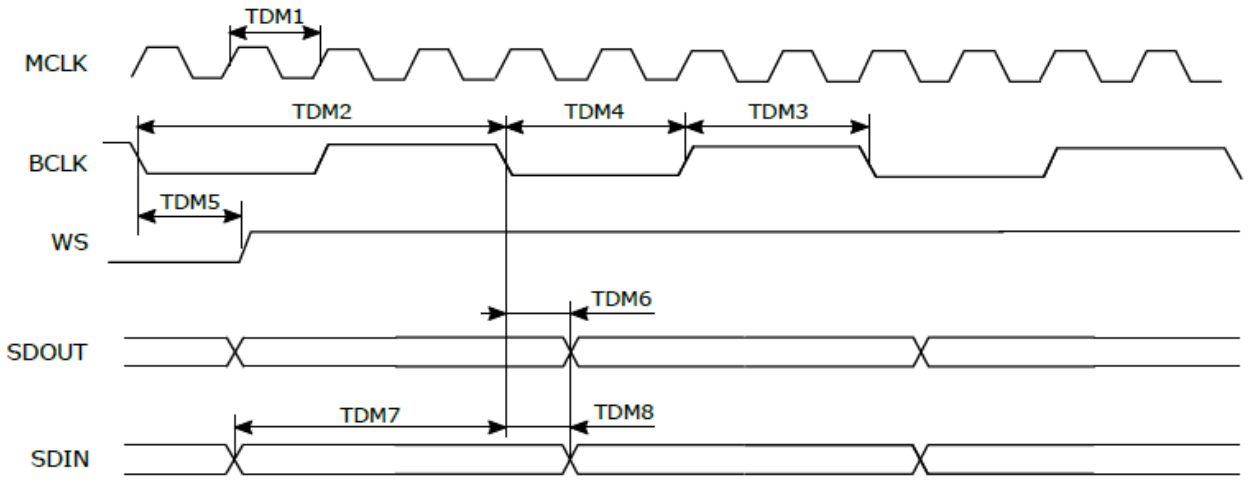


Figure 3-16 TDM Master Mode Timing Diagram

3.10.4 Pulse Density Modulation (PDM)

The PDM module includes the following key features:

- Supports one stereo DMIC over one data wire
- Supports audio sampling rates of 8, 16, 32, 48 KHz

3.10.4.1 PDM Timing Characteristics

Table 3-32 and Figure 3-17 present timing characteristics for PDM interface in the device.

Table 3-32 PDM Timing Characteristics

No.	Parameter	Description	Min	Typ	Max	Unit
PDM1	f_{OP}	Operating frequency, PDM CLK	0.40625	-	3.25	MHz
PDM2	$t_{W\_CLK\_H}$	Pulse duration, CLK high	-	0.5	-	1 / f_{CLK}
PDM3	$t_{W\_CLK\_L}$	Pulse duration, CLK low	-	0.5	-	1 / f_{CLK}
PDM4	t_{SU_DAT}	Setup time, DAT	20	-	-	ns
PDM5	t_{H_DAT}	Hold time, DAT	20	-	-	ns

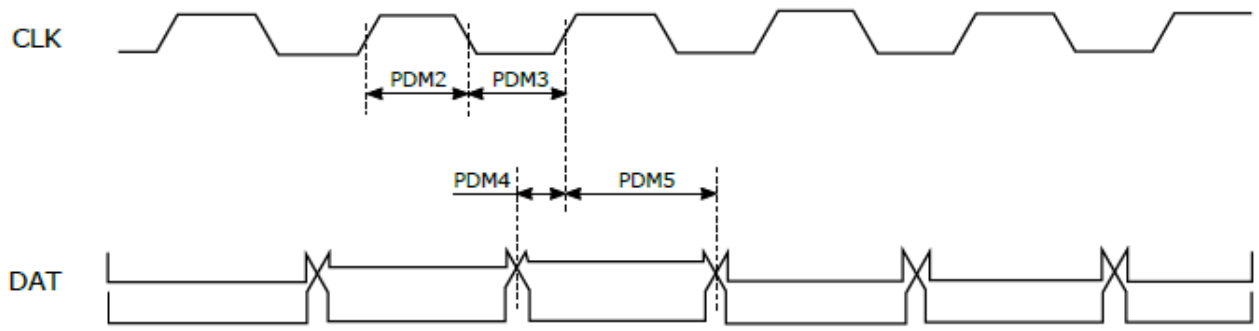


Figure 3-17 PDM Timing Diagram

3.10.4.2 DMIC Signal Descriptions

Table 3-33 presents DMIC signal descriptions.

Table 3-33 DMIC Signal Descriptions

Signal Name	Type	Description	Ball Location
DMIC_CLK	DO	DMIC clock	AC26, AF23, L5, Y22
DMIC_DAT	DI	PDM data input from DMIC	AC25, AF26, K5, , AA22

3.10.4.3 DMIC Filter Characteristics

Table 3-34 presents filter characteristics for the DMIC interface in the device.

Table 3-34 DMIC Filter Characteristics

Parameter	Description	Min	Typ	Max	Unit
f_{OP}	Operating frequency		3.25 1.625 0.8125 0.40625		MHz

Parameter	Description	Min	Typ	Max	Unit
D	Duty cycle, CLK	40		60	%
t_{RISE}	Rise time, CLK (Max C_L = 80 pF)		10		ns
t_{FALL}	Fall time, CLK (Max C_L = 80 pF)		10		ns
f_S	Audio sampling rate	8		48	kHz

3.11 Analog Baseband

The Analog Baseband (ABB) interface is a common control interface for communication with the analog blocks in the device.

3.11.1 ABB Signal Descriptions

Table 3-35 presents ABB signal descriptions.

Table 3-35 ABB Signal Descriptions

Signal Name	Type	Description	Ball Location
APC	AIO	Automatic power control	AE13
Detection path			
DET_IN0	AIO	RF0 IN detection path	AJ12
DET_IN1	AIO	RF1 IN detection path	AH11
DET_IP0	AIO	RF0 IP detection path	AJ13
DET_IP1	AIO	RF1 IP detection path	AH12
DET_QN0	AIO	RF0 QN detection path	AH13
DET_QN1	AIO	RF1 QN detection path	AJ10
DET_QP0	AIO	RF0 QP detection path	AH14
DET_QP1	AIO	RF1 QP detection path	AH10
Diverse downlink			
DRX_BB_I0	AIO	Diverse downlink I-ch for path 0	AH16
DRX_BB_I1	AIO	Diverse downlink I-ch for path 1	AG17
DRX_BB_Q0	AIO	Diverse downlink Q-ch for path 0	AH17
DRX_BB_Q1	AIO	Diverse downlink Q-ch for path 1	AF17
PRX_BB_I0	AIO	Main downlink I-ch for path 0	AJ16
PRX_BB_I1	AIO	Main downlink I-ch for path 1	AF16
PRX_BB_Q0	AIO	Main downlink Q-ch for path 0	AJ15
PRX_BB_Q1	AIO	Main downlink Q-ch for path 1	AG16
DAC			
RFIC_ET0_N	AIO	Envelop tracking DAC0 negative output	AE12
RFIC_ET0_P	AIO	Envelop tracking DAC0 positive output	AE11
Uplink path			
TX_BB_IN0	AIO	Uplink IN for path0	AG13
TX_BB_IN1	AIO	Uplink IN for path1	AF11
TX_BB_IP0	AIO	Uplink IP for path0	AF13
TX_BB_IP1	AIO	Uplink IP for path1	AG11
TX_BB_QN0	AIO	Uplink QN for path0	AG14
TX_BB_QN1	AIO	Uplink QN for path1	AG12
TX_BB_QP0	AIO	Uplink QP for path0	AF14

Signal Name	Type	Description	Ball Location
TX_BB_QP1	AIO	Uplink QP for path1	AF12
Voice wakeup			
VOW_CLK_MISO	DI	Voice wakeup interface	L23
VOW_DAT_MISO	DI	Voice wakeup interface	N24

3.11.2 PMIC Audio Interface Signal Descriptions

Table 3-36 presents PMIC audio interface signal descriptions.

Table 3-36 PMIC Signal Descriptions

Signal Name	Type	Description	Ball Location
AUD_CLK_MISO	DI	PMIC audio interface clock master input	M24, M25
AUD_CLK_MOSI	DO	PMIC audio interface clock master output	M24, M25
AUD_DAT_MISO0	DI	PMIC audio interface data master input	J22, N24
AUD_DAT_MISO1	DI	PMIC audio interface data master input	N27, L23
AUD_DAT_MOSI0	DO	PMIC audio interface data master output	J22, N24
AUD_DAT_MOSI1	DO	PMIC audio interface data master output	N27, L23
AUD_SYNC_MISO	DI	PMIC audio interface sync master input	L26, M26
AUD_SYNC_MOSI	DO	PMIC audio interface sync master output	L26, M26

3.12 Connectivity

3.12.1 Inter-Integrated Circuit (I2C)

The device contains nine I2C controllers providing interface between internal hosts and any I^{2}C™ bus compatible device. Each can be configured to work as a master I^{2}C-compatible device.

Each I2C module supports the following key features:

- Compliant with Philips I^{2}C-bus Specification version 2.1
- Standard-Speed (SS) communication mode (up to 100 Kbps)
- Fast-Speed (FS) communication mode (up to 400 Kbps)
- High-Speed (HS) communication mode (up to 3.4 Mbps)
- 7- or 10-bit addressing
- START/STOP/REPEATED START conditions
- Adjustable clock speed for SS and FS modes of operation
- Manual transfer mode
- Multi-write per transfer
- Multi-read per transfer
- Multi-transfer per transaction
- Combined format transfer with length change capability
- Repeated start multiple transfer

The following I2C modules support other bus modes in addition to the standard I2C:

- I2C1: Support for I^{3}C (SDR mode only)

- I2C2: Support for I^3C (SDR mode only) and SCCB (Serial Camera Control Bus)
- I2C4: Support for I^3C (SDR mode only) and SCCB

3.12.1.1 I2C Signal Descriptions

Table 3-37 presents I2C signal descriptions.

Table 3-37 I2C Signal Descriptions

Signal Name	Type	Description	Ball Location
I2C0(1)			
SCL0	DIO	I2C0 serial clock (input/output)	AB6
SDA0	DIO	I2C0 serial data (input/output)	AC5
I2C1(1)			
SCL1	DIO	I2C1 serial clock (input/output)	AE4, AF3, AA22
SDA1	DIO	I2C1 serial data (input/output)	AF4, AH2, Y22
I2C2(1)			
SCL2	DIO	I2C2 serial clock (input/output)	AB2
SDA2	DIO	I2C2 serial data (input/output)	AB1
I2C3(1)			
SCL3	DIO	I2C3 serial clock (input/output)	AF22
SDA3	DIO	I2C3 serial data (input/output)	AG22
I2C4(1)			
SCL4	DIO	I2C4 serial clock (input/output)	Y2
SDA4	DIO	I2C4 serial data (input/output)	W2
I2C5(1)			
SCL5	DIO	I2C5 serial clock (input/output)	AH24
SDA5	DIO	I2C5 serial data (input/output)	AH25
I2C6(2)			
SCL6	DIO	I2C6 serial clock (input/output)	AG2, N26, Y23, J4, T23
SDA6	DIO	I2C6 serial data (input/output)	AG1, P26, AA24, J5, R22
I2C7(2)			
SCL7	DIO	I2C7 serial clock (input/output)	AD4, AC26, L3, AG23
SDA7	DIO	I2C7 serial data (input/output)	AC25, L5, K3, AD21
I2C8(2)			
SCL8	DIO	I2C8 serial clock (input/output)	AA6, K4, AG21
SDA8	DIO	I2C8 serial data (input/output)	W5, K5, AD20

1. I2C0 to I2C5 have default HW internal 5 kΩ pull-up changed by the SW initialization to 1 kΩ.
2. I2C6 to I2C8 must be connected to an external pull-up 4.7 kΩ for SS and FS modes, and to an external pull-up 2.2 kΩ for HS mode.

3.12.1.2 I2C Timing Characteristics

Table 3-38 and Figure 3-18 present timing characteristics for I2C interfaces in SS/FS/FS+ modes.

Table 3-38 I2C Timing Characteristics (SS/FS/FS+ modes)

No.	Parameter		SS		FS		FS+		Unit
			Min	Max	Min	Max	Min	Max	
	t_c	Cycle time		10000		2500		1000	ns
IIC2	$t_{w\ high}$	Pulse duration, SCL high	4.0		0.6		0.26		µs
IIC3	$t_{w\ low}$	Pulse duration, SCL low	4.7		1.3		0.5		µs
IIC4	t_{RISE}	Rise time of SDA and SCL signals		100	20	300		120	ns
IIC5	t_{FALL}[1]	Fall time of SDA and SCL signals		300	20 × (VDD / 5.5 V)	300	20 × (VDD / 5.5 V)	120	ns
IIC6	t_{su}	Setup time, SDA to SCL	250		100		50		ns
IIC7	t_h[2]	Hold time, SDA to SCL	5.0		0		0		µs
IIC8	$t_{su\ start}$	Setup time, SCL to repeated START (Sr) condition	4.7		0.6		0.26		µs
IIC9	$t_{h\ start}$	Hold time, START (S) condition to SCL	4.0		0.6		0.26		µs
IIC10	$t_{h\ stop}$	Setup time, SCL to STOP (P) condition	4.0		0.6		0.26		ns
IIC11	$t_{(BUF)}$	Bus free time between STOP (P) and START (S) condition	4.7		1.3		0.5		ns
IIC12	t_{DV}	Data valid time		3.45		0.9		0.45	µs
IIC13	t_{DV_ACK}	Data valid acknowledge time		3.45		0.9		0.45	µs

1. VDD: I2C IO voltage
2. I2C-bus devices

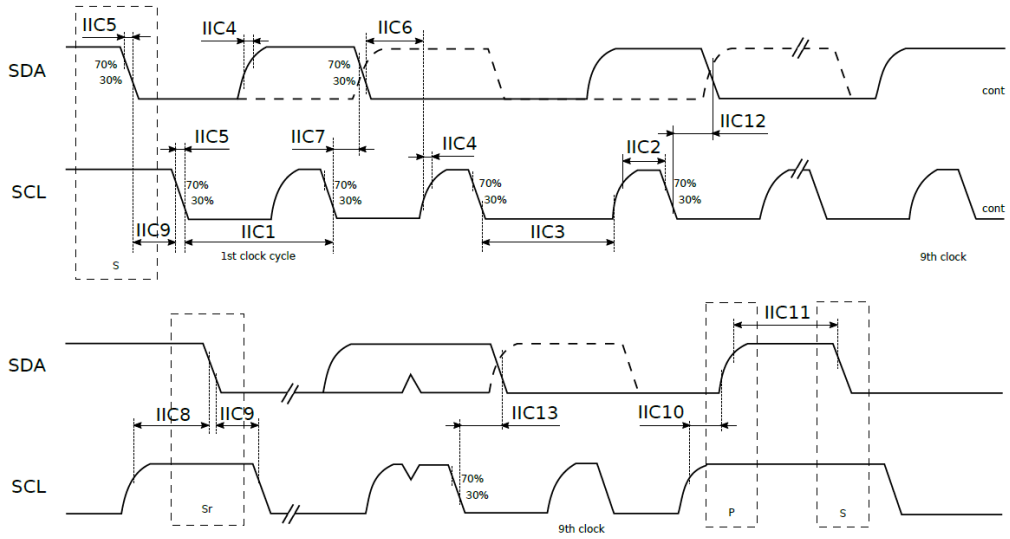


Figure 3-18 I2C Timing Diagram (SS/FS/FS+ modes)

Table 3-39 I2C Timing Characteristics (HS mode)

No.	Parameter		Cb = 100 pF (max)		Cb = 400 pF (max)		Unit
			Min	Max	Min	Max	
IIC1	t_c	Cycle time	0	294	0	588	ns
IIC2	$t_{su\ start}$	Setup time, SCL to repeated START condition	160		160		ns
IIC3	$t_{h\ start}$	Hold time, (repeated) START condition to SCL	160		160		ns
IIC4	$t_{w\ low}$	Pulse duration, SCL low	160		320		ns
IIC5	$t_{w\ high}$	Pulse duration, SCL high	60		120		ns
IIC6	t_h[(1)]	Hold time, SDA to SCL	0	70	0	150	ns
IIC7	t_{su}	Setup time, SDA to SCL	10		10		ns
IIC8	t_{RISE}	Rise time of SDA and SCL signals	10	40	20	80	ns
IIC9	t_{FALL}	Fall time of SDA and SCL signals	10	40	20	80	ns
IIC10	$t_{h\ stop}$	Setup time, SCL to STOP condition	160		160		ns

1. I2C-bus devices

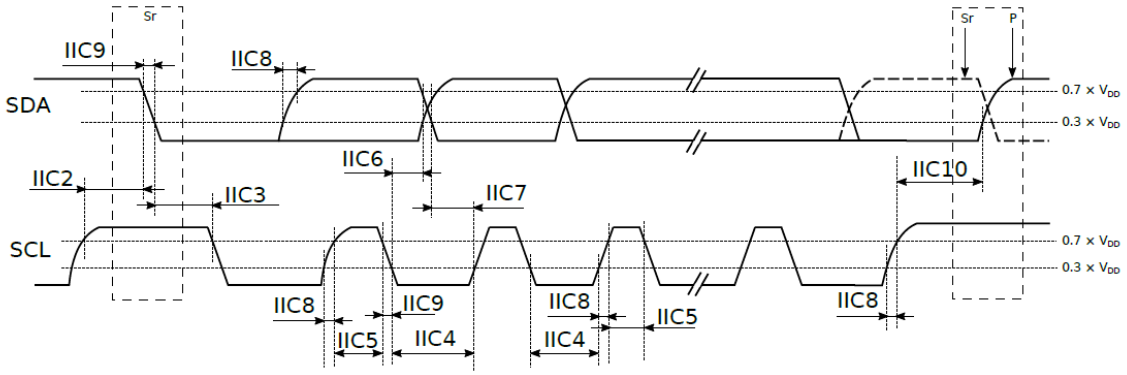


Figure 3-19 I2C Timing Diagram (HS mode)

3.12.2 Universal Asynchronous Receiver/Transmitter (UART)

The device supports two UART modules, which provide full-duplex serial communication with external devices.

Each UART module supports the following key features:

- 16C450-compatible
- 16550A-compatible
- Fully programmable by an 8-bit CPU interface
- Configurable data formats:
  - 5, 6, 7, or 8 data bits
  - Optional parity bit
  - 1 or 2 stop bits
- Internal 16-bit programmable baud rate generator
- 8-bit scratch register
- Separate transmit and receive FIFOs
- Baud rates from 110 bps up to 961,200 bps
- Baud rate auto detection function
- Two DMA handshake lines
- Polling, DMA and interrupt modes of operation

- Hardware flow control (RTS/CTS)

3.12.2.1 UART Signal Descriptions

Table 3-40 presents UART signal descriptions.

Table 3-40 UART Signal Descriptions

Signal Name	Type	Description	Ball Location
UART0			
UCTS0	DI	UART0 clear to send (active low)	N26, AF23, W6, AD20
URTS0	DO	UART0 request to send (active low)	P26, AF26, Y5, AG19
URXD0	DI	UART0 receive data	AD2, AD1
UTXD0	DO	UART0 transmit data	AD2, AD1
UART1			
UCTS1	DI	UART1 clear to send (active low)	N26, AA26, AG25
URTS1	DO	UART1 request to send (active low)	P26, AA23, AG24
URXD1	DI	UART1 receive data	W24, AF23, AG25, L3, H3, AD21
UTXD1	DO	UART1 transmit data	Y24, AF26, AG24, K3, H4, AG21

3.12.3 Serial Peripheral Interface (SPI)

The SPI is a four-pin synchronous serial interface used for short-distance communication, primarily in embedded systems. The device features six SPI master controllers.

The SPI supports the following key features:

- Two configurable transmit modes:
  - TX DMA mode—the SPI controller automatically fetches the transmission data to be put on the MOSI line from memory.
  - TX FIFO mode—the transmission data to be put on the MOSI line are written to a FIFO before the start of the transaction.
- Two configurable receive modes:
  - RX DMA mode—the SPI controller automatically stores the received data (from MISO line) to memory.
  - RX FIFO mode—the received data is kept in an RX FIFO of the SPI controller. The processor must read the data.
- Configurable chip-select setup, hold, and idle time
- Programmable serial clock (SCK) high and low time
- Configurable transmit and receive bit order
- Adjustable endian order from/to memory system
- Programmable byte length for transmission
- Unlimited length for transmission using dedicated pause mode
- Configurable option to control chip-select de-assertion between byte transfers
- Supports all clock polarity and phase modes

3.12.3.1 SPI Signal Descriptions

Table 3-41 presents SPI signal descriptions.

Table 3-41 SPI Signal Descriptions

Signal Name	Type	Description	Ball Location
SPI0			
SPI0_CLK	DO	SPI0 serial clock	AF3
SPI0_CSB	DO	SPI0 chip select, active low	AG3
SPI0_MI	DI	SPI0 master input / slave output	AJ2
SPI0_MO	DO	SPI0 master output / slave input	AH2
SPI1			
SPI1_A_CLK	DO	SPI1 serial clock (channel A)	AA22
SPI1_A_CSB	DO	SPI1 chip select (channel A), active low	AB25
SPI1_A_MI	DI	SPI1 master input / slave output (channel A)	W22
SPI1_A_MO	DO	SPI1 master output / slave input (channel A)	Y22
SPI1_B_CLK	DO	SPI1 serial clock (channel B)	Y4
SPI1_B_CSB	DO	SPI1 chip select (channel B), active low	AD4
SPI1_B_MI	DI	SPI1 master input / slave output (channel B)	AE1
SPI1_B_MO	DO	SPI1 master output / slave input (channel B)	W4
SPI2			
SPI2_CLK	DO	SPI2 serial clock	AG2
SPI2_CSB	DO	SPI2 chip select, active low	AB5
SPI2_MI	DI	SPI2 master input / slave output	AE3
SPI2_MO	DO	SPI2 master output / slave input	AB4
SPI3			
SPI3_CLK	DO	SPI3 serial clock	AA23
SPI3_CSB	DO	SPI3 chip select, active low	Y26
SPI3_MI	DI	SPI3 master input / slave output	AB24
SPI3_MO	DO	SPI3 master output / slave input	AA26
SPI4			
SPI4_CLK	DO	SPI4 serial clock	Y24
SPI4_CSB	DO	SPI4 chip select, active low	AB23
SPI4_MI	DI	SPI4 master input / slave output	AB26
SPI4_MO	DO	SPI4 master output / slave input	W24
SPI5			
SPI5_CLK	DO	SPI5 serial clock	W26
SPI5_CSB	DO	SPI5 chip select, active low	AA25
SPI5_MI	DI	SPI5 master input / slave output	W23
SPI5_MO	DO	SPI5 master output / slave input	W25

3.12.3.2 SPI Timing Characteristics

Table 3-42 and Figure 3-20 present timing characteristics for SPI in the device.

Table 3-42 SPI Timing Characteristics

No.	Parameter		Min	Typ	Unit
	f_{OP_MCK}	SPI HW module clock frequency (MCK)—chip internal clock		55	MHz
SPI02	t_c	Cycle time, SPI_CLK	18.2(1)		ns
SPI05	$t_{w\_CLK\_L}$	Pulse duration, SPI_CLK low	9.1		ns

No.	Parameter		Min	Typ	Unit
SPI06	$t_{w\_CLK\_H}$	Pulse duration, SPI_CLK high	9.1		ns
SPI07	t_{su_cs}	Setup time, SPI_CSB—register adjustable			ns
SPI08	t_{h_cs}	Hold time, SPI_CSB—register adjustable	9.1		ns
SPI09	t_{su_MOSI}	Setup time, SPI_MO to SPI_CLK	0		ns

1. For maximum operating clock frequency refer to Table 6-1.

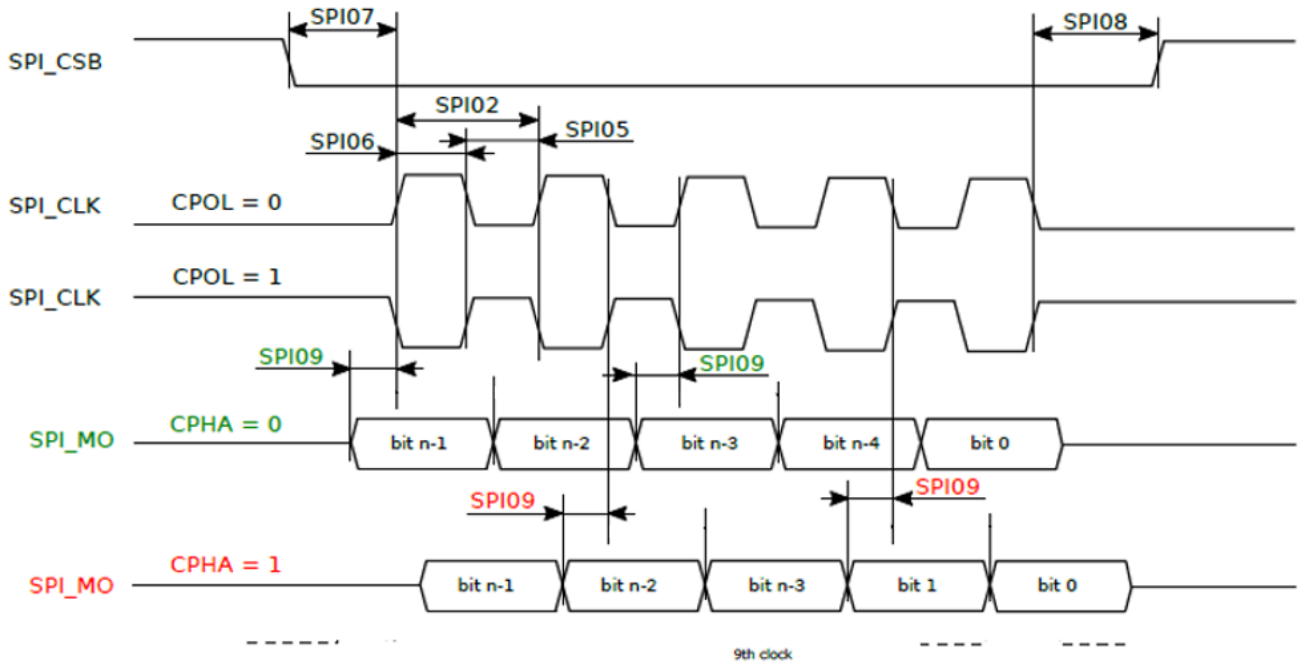


Figure 3-20 SPI Master Timing Diagram

3.12.4 SuperSpeed Universal Serial Bus (SSUSB)

The device features one USB module with an xHCI host controller, a device controller (USB3.0) and two integrated MAC/PHY—one High-Speed (HS) / Full-Speed (FS) and one SuperSpeed (SS).

The USB controller has the following key features:

- Supports USB3.0 in static device role
- Supports host role and Dual-Role-Device (DRD) in USB2.0 mode
- Shared hardware when in DRD mode
- Proprietary application layer device controller with linked list queue and scatter/gather DMA
- Support of xHCI-based host controller
- Support of embedded SS PHY with 32-bit @ 125 MHz PIPE interface
- Support of embedded HS/FS PHY with 16-bit @ 30 MHz UTMI interface
- HS/FS OTG DRD compliant with OTG Supplement Version 2.0

3.12.4.1 SSUSB Signal Descriptions

Table 3-43 presents USB signal descriptions.

Table 3-43 SSUSB Signal Descriptions

Signal Name	Type	Description	Ball Location
CHD_DM	AIO	BC1.1 charger mode detection D-	G24

Signal Name	Type	Description	Ball Location
CHD_DP	AIO	BC1.1 charger mode detection D+	G25
IDDIG	DI	USB OTG ID. Cable end detector: • GND: micro-A • Floating: micro-B	AE2, N26, AF23, AG25, W6, K3, T23, W22
SSUSB_RXN	AI	USB SuperSpeed receive data negative	J27
SSUSB_RXP	AI	USB SuperSpeed receive data positive	H27
SSUSB_TXN	AO	USB SuperSpeed transmit data negative	J24
SSUSB_TXP	AO	USB SuperSpeed transmit data positive	J25
USB_DM	AIO	USB D- bi-directional differential data	F26
USB_DP	AIO	USB D+ bi-directional differential data	G26
USB_DRVVBUS	DO	USB VBUS—signal to external power switch enable	AE1, P26, AF26, AG24, Y5, L3, R22, AB25

3.12.5 KeyPad Scanner (KeyPad)

The KeyPad implements scanning algorithm for hardware-based key-press decoding and reduces overhead to the CPU.

The KeyPad supports the following key features:

- Two types of keyboards:
  - 3 × 3 single keys
  - 3 × 3 configurable double keys
- Key detection block providing key pressed, key released and de-bounce mechanisms
- Interrupt event detection on key press and key release
- Detection of one or two keys pressed simultaneously with any combination

3.12.5.1 KeyPad Signal Descriptions

Table 3-44 presents KeyPad signal descriptions.

Table 3-44 KeyPad Signal Descriptions

Signal Name	Type	Description	Ball Location
KPCOL0	DIO	KeyPad column 0	AC4
KPCOL1	DIO	KeyPad column 1	AE3
KPCOL2	DIO	KeyPad column 2	Y23, L3, T23, W22
KPROW0	DIO	KeyPad row 0	AA5
KPROW1	DIO	KeyPad row 1	AH1
KPROW2	DIO	KeyPad row 2	AA24, K3, R22, AB25

3.12.5.2 KeyPad Applications

The KeyPad supports a 3 × 3 keys matrix.

NOTE: KeyPad does not support detection of simultaneously pressed keys on the same column and row.

Figure 3-21 represents 3 × 3 double KeyPad matrix example configuration.

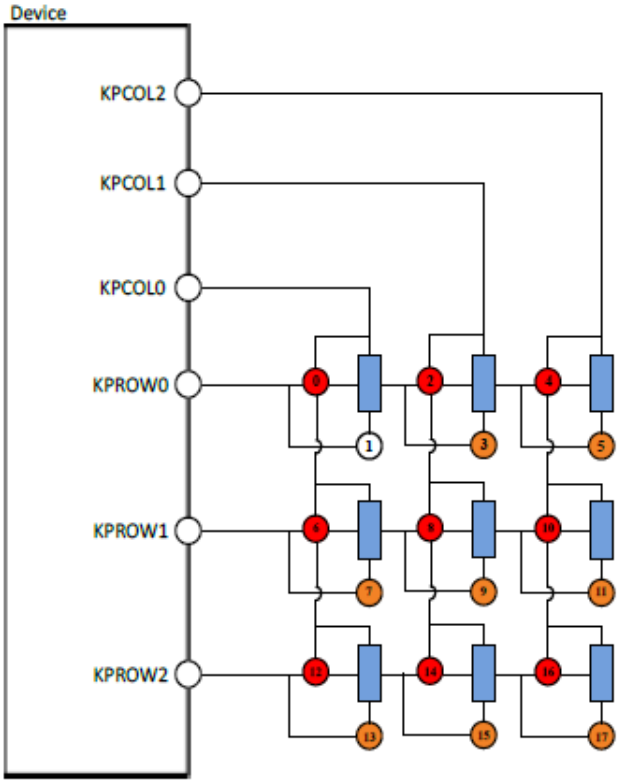


Figure 3-21 KeyPad Double Key Matrix

3.12.6 General Purpose I/O (GPIO)

The GPIO peripheral provides 180 dedicated GPIO pins, multiplexed with other functions to reduce the pin count.

Each GPIO pin has the following key functions:

- Configurable direction: input or output
- Control of the state driven on the output pin when GPIO is configured as an output
- Detection of the state of the pin when GPIO is configured as an input
- Configurable interrupt event generation

3.12.6.1 GPIO Signal Descriptions

Table 3-45 presents GPIO signal descriptions.

Table 3-45 GPIO Signal Descriptions

Signal Name	Type	Description	Ball Location
GPIO0	DIO	General purpose input and output	AB5
GPIO1	DIO	General purpose input and output	AB4
GPIO2	DIO	General purpose input and output	AG2
GPIO3	DIO	General purpose input and output	AG1
GPIO4	DIO	General purpose input and output	AC3
GPIO5	DIO	General purpose input and output	AF2
GPIO6	DIO	General purpose input and output	AE2
GPIO7	DIO	General purpose input and output	AE1
GPIO8	DIO	General purpose input and output	AD4
GPIO9	DIO	General purpose input and output	W4

Signal Name	Type	Description	Ball Location
GPIO10	DIO	General purpose input and output	Y4
GPIO11	DIO	General purpose input and output	N26
GPIO12	DIO	General purpose input and output	P26
GPIO13	DIO	General purpose input and output	W23
GPIO14	DIO	General purpose input and output	AA25
GPIO15	DIO	General purpose input and output	W25
GPIO16	DIO	General purpose input and output	W26
GPIO17	DIO	General purpose input and output	AB26
GPIO18	DIO	General purpose input and output	AB23
GPIO19	DIO	General purpose input and output	W24
GPIO20	DIO	General purpose input and output	Y24
GPIO21	DIO	General purpose input and output	AB24
GPIO22	DIO	General purpose input and output	Y26
GPIO23	DIO	General purpose input and output	AA26
GPIO24	DIO	General purpose input and output	AA23
GPIO25	DIO	General purpose input and output	Y23
GPIO26	DIO	General purpose input and output	AA24
GPIO27	DIO	General purpose input and output	AC26
GPIO28	DIO	General purpose input and output	AC25
GPIO29	DIO	General purpose input and output	AC24
GPIO30	DIO	General purpose input and output	AD27
GPIO31	DIO	General purpose input and output	AD26
GPIO32	DIO	General purpose input and output	AD24
GPIO33	DIO	General purpose input and output	AC23
GPIO34	DIO	General purpose input and output	AE26
GPIO35	DIO	General purpose input and output	AE24
GPIO36	DIO	General purpose input and output	AE25
GPIO37	DIO	General purpose input and output	AD23
GPIO38	DIO	General purpose input and output	AE23
GPIO39	DIO	General purpose input and output	AE22
GPIO40	DIO	General purpose input and output	AF24
GPIO41	DIO	General purpose input and output	AF23
GPIO42	DIO	General purpose input and output	AF26
GPIO43	DIO	General purpose input and output	AH23
GPIO44	DIO	General purpose input and output	AG26
GPIO45	DIO	General purpose input and output	AH27
GPIO46	DIO	General purpose input and output	AG25
GPIO47	DIO	General purpose input and output	AG24
GPIO48	DIO	General purpose input and output	AH24
GPIO49	DIO	General purpose input and output	AH25
GPIO50	DIO	General purpose input and output	AF22
GPIO51	DIO	General purpose input and output	AG22
GPIO52	DIO	General purpose input and output	AJ25
GPIO53	DIO	General purpose input and output	AJ24
GPIO54	DIO	General purpose input and output	AH26

Signal Name	Type	Description	Ball Location
GPIO55	DIO	General purpose input and output	AJ26
GPIO56	DIO	General purpose input and output	AH22
GPIO57	DIO	General purpose input and output	AJ22
GPIO58	DIO	General purpose input and output	AG20
GPIO59	DIO	General purpose input and output	AE20
GPIO60	DIO	General purpose input and output	AF20
GPIO61	DIO	General purpose input and output	AG7
GPIO62	DIO	General purpose input and output	AH7
GPIO63	DIO	General purpose input and output	AJ8
GPIO64	DIO	General purpose input and output	AJ7
GPIO65	DIO	General purpose input and output	AE6
GPIO66	DIO	General purpose input and output	AD6
GPIO67	DIO	General purpose input and output	AG6
GPIO68	DIO	General purpose input and output	AF6
GPIO69	DIO	General purpose input and output	AH6
GPIO70	DIO	General purpose input and output	AJ5
GPIO71	DIO	General purpose input and output	AD5
GPIO72	DIO	General purpose input and output	AE5
GPIO73	DIO	General purpose input and output	AF5
GPIO74	DIO	General purpose input and output	AG5
GPIO75	DIO	General purpose input and output	AH5
GPIO76	DIO	General purpose input and output	AC6
GPIO77	DIO	General purpose input and output	AJ4
GPIO78	DIO	General purpose input and output	AH4
GPIO79	DIO	General purpose input and output	AG4
GPIO80	DIO	General purpose input and output	AH3
GPIO81	DIO	General purpose input and output	AF4
GPIO82	DIO	General purpose input and output	AC5
GPIO83	DIO	General purpose input and output	AB6
GPIO84	DIO	General purpose input and output	AE4
GPIO85	DIO	General purpose input and output	AJ2
GPIO86	DIO	General purpose input and output	AG3
GPIO87	DIO	General purpose input and output	AH2
GPIO88	DIO	General purpose input and output	AF3
GPIO89	DIO	General purpose input and output	W5
GPIO90	DIO	General purpose input and output	AA6
GPIO91	DIO	General purpose input and output	AH1
GPIO92	DIO	General purpose input and output	AA5
GPIO93	DIO	General purpose input and output	AC4
GPIO94	DIO	General purpose input and output	AE3
GPIO95	DIO	General purpose input and output	AD2
GPIO96	DIO	General purpose input and output	AD1
GPIO97	DIO	General purpose input and output	W6
GPIO98	DIO	General purpose input and output	Y5
GPIO99	DIO	General purpose input and output	AA4

Signal Name	Type	Description	Ball Location
GPIO100	DIO	General purpose input and output	AC2
GPIO101	DIO	General purpose input and output	AA3
GPIO102	DIO	General purpose input and output	AA2
GPIO103	DIO	General purpose input and output	AB2
GPIO104	DIO	General purpose input and output	AB1
GPIO105	DIO	General purpose input and output	Y2
GPIO106	DIO	General purpose input and output	W2
GPIO107	DIO	General purpose input and output	L5
GPIO108	DIO	General purpose input and output	K4
GPIO109	DIO	General purpose input and output	K5
GPIO110	DIO	General purpose input and output	L3
GPIO111	DIO	General purpose input and output	L4
GPIO112	DIO	General purpose input and output	K3
GPIO113	DIO	General purpose input and output	J4
GPIO114	DIO	General purpose input and output	J5
GPIO115	DIO	General purpose input and output	H4
GPIO116	DIO	General purpose input and output	H5
GPIO117	DIO	General purpose input and output	J6
GPIO118	DIO	General purpose input and output	J7
GPIO119	DIO	General purpose input and output	H6
GPIO120	DIO	General purpose input and output	K6
GPIO121	DIO	General purpose input and output	H3
GPIO122	DIO	General purpose input and output	C27
GPIO123	DIO	General purpose input and output	B26
GPIO124	DIO	General purpose input and output	D24
GPIO125	DIO	General purpose input and output	A26
GPIO126	DIO	General purpose input and output	C26
GPIO127	DIO	General purpose input and output	G23
GPIO128	DIO	General purpose input and output	B27
GPIO129	DIO	General purpose input and output	C25
GPIO130	DIO	General purpose input and output	D26
GPIO131	DIO	General purpose input and output	E25
GPIO132	DIO	General purpose input and output	E24
GPIO133	DIO	General purpose input and output	D25
GPIO134	DIO	General purpose input and output	K26
GPIO135	DIO	General purpose input and output	M23
GPIO136	DIO	General purpose input and output	M24
GPIO137	DIO	General purpose input and output	L26
GPIO138	DIO	General purpose input and output	J22
GPIO139	DIO	General purpose input and output	N27
GPIO140	DIO	General purpose input and output	M25
GPIO141	DIO	General purpose input and output	M26
GPIO142	DIO	General purpose input and output	N24
GPIO143	DIO	General purpose input and output	L23
GPIO144	DIO	General purpose input and output	P24

Signal Name	Type	Description	Ball Location
GPIO145	DIO	General purpose input and output	N23
GPIO146	DIO	General purpose input and output	P25
GPIO147	DIO	General purpose input and output	P23
GPIO148	DIO	General purpose input and output	R23
GPIO149	DIO	General purpose input and output	R24
GPIO150	DIO	General purpose input and output	R25
GPIO151	DIO	General purpose input and output	L25
GPIO152	DIO	General purpose input and output	M22
GPIO153	DIO	General purpose input and output	L22
GPIO154	DIO	General purpose input and output	N25
GPIO155	DIO	General purpose input and output	P22
GPIO156	DIO	General purpose input and output	T23
GPIO157	DIO	General purpose input and output	R22
GPIO158	DIO	General purpose input and output	N22
GPIO159	DIO	General purpose input and output	T22
GPIO160	DIO	General purpose input and output	K22
GPIO161	DIO	General purpose input and output	W22
GPIO162	DIO	General purpose input and output	AB25
GPIO163	DIO	General purpose input and output	Y22
GPIO164	DIO	General purpose input and output	AA22
GPIO165	DIO	General purpose input and output	Y25
GPIO166	DIO	General purpose input and output	V22
GPIO167	DIO	General purpose input and output	AE21
GPIO168	DIO	General purpose input and output	AF21
GPIO169	DIO	General purpose input and output	AD25
GPIO170	DIO	General purpose input and output	AG23
GPIO171	DIO	General purpose input and output	AD21
GPIO172	DIO	General purpose input and output	AG21
GPIO173	DIO	General purpose input and output	AD20
GPIO174	DIO	General purpose input and output	AG19
GPIO175	DIO	General purpose input and output	AD22
GPIO176	DIO	General purpose input and output	AD19
GPIO177	DIO	General purpose input and output	AA7
GPIO178	DIO	General purpose input and output	Y7
GPIO179	DIO	General purpose input and output	Y6

3.12.7 Pulse Width Modulation (PWM)

The device features three generic PWM modules to generate pulse sequences with programmable frequency and duration for a variety of applications.

Each PWM module supports the following key features:

- Old mode, FIFO mode
- Periodical memory and random modes
- Sequential output mode

3.12.7.1 PWM Signal Descriptions

Table 3-46 presents PWM signal descriptions.

Table 3-46 PWM Signal Descriptions

Signal Name	Type	Description	Ball Location
PWM_A	DO	PWM output A	AE2, AA6, L5, R25, L22
PWM_B	DO	PWM output B	AC3, AG20, AH1, K4, L25, Y25
PWM_C	DO	PWM output C	AF2, W5, AC2, K5, M22, AD25

3.12.7.2 PWM Timing Characteristics

Table 3-47 and Figure 3-22 present timing characteristics for PWM interfaces in the device.

Table 3-47 PWM Timing Characteristics

No.	Parameter	
PWM01	t_c	Cycle time
PWM02	t_w	Pulse duration, PWM

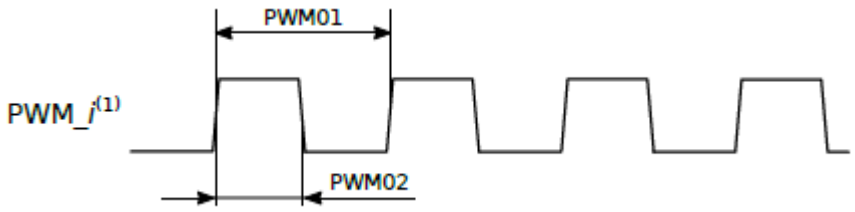


Figure 3-22 PWM Timing Diagram

1. In this diagram, *i* stands for A, B, or C.

3.13 Wireless Connectivity

The device supports four wireless connectivity functions, WLAN, BT, GPS, and FM, with RF parts integrated in the MT6631, MT7668 chips. With the built-in advanced and sophisticated radio coexistence algorithms and hardware mechanisms, the device provides the best and most convenient connectivity solution among the industry. The small footprint with low-power consumption greatly reduces the PCB layout resource.

The Wireless Communication Module (WCM) supports the following key features:

- Advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms
- Single shared antenna for BT, WLAN, and GNSS
- Single Temperature-Compensated Crystal Oscillator (TCXO) and Thermistor Crystal (TMS) for BT, WLAN, and GNSS
- Self-calibration
- Intelligent BT/WLAN coexistence scheme
- Best-in-class current consumption performance

The WCM is programmed only by CPU internal API and Wireless Management Task (WMT). Therefore the user does not need to individually set-up the WCM.

3.13.1 WCM Signal Descriptions

Table 3-48 presents WCM signal descriptions.

Table 3-48 WCM Signal Descriptions

Signal Name	Type	Description	Ball Location
AGPS_SYNC	DO	Assisted GNSS synchronization	K3, D25, AD25
CONN_BT_CLK	DIO	MT6631 BT 2-wire interface	H4
CONN_BT_DATA	DIO	MT6631 BT 2-wire interface	H5
CONN_HRST_B	DO	MT6631 reset	H3
CONN_TOP_CLK	DO	MT6631 TOP 2-wire interface	J4
CONN_TOP_DATA	DIO	MT6631 TOP 2-wire interface	J5
CONN_WB_PTA	DIO	MT6631 Wi-Fi / BT PTA	K6
CONN_WF_HB0	DIO	MT6631 Wi-Fi 3-wire interface	J6
CONN_WF_HB1	DIO	MT6631 Wi-Fi 3-wire interface	J7
CONN_WF_HB2	DIO	MT6631 Wi-Fi 3-wire interface	H6
BT_IN	AIO	BT I-channel negative-end	F1
BT_IP	AIO	BT I-channel positive-end	F2
BT_QN	AIO	BT Q-channel negative-end	G2
BT_QP	AIO	BT Q-channel positive-end	G1
GPS_I	AIO	GPS I-channel	J2
GPS_Q	AIO	GPS Q-channel	J1
WF_IN	AIO	Wi-Fi I-channel negative-end	C1
WF_IP	AIO	Wi-Fi I-channel positive-end	B1
WF_QN	AIO	Wi-Fi Q-channel negative-end	D2
WF_QP	AIO	Wi-Fi Q-channel positive-end	D1
XIN_WBG	AIO	WBG crystal clock input	H8

3.13.2 Wireless Local Area Network (WLAN)

The WLAN module includes the following key features:

- Dual-band (2.4 GHz and 5 GHz) single stream 802.11 ac/a/b/g/n MAC/BB/RF)
- Compliance with 802.11 d/e/h/i/j/k/r/v
- Security: WFA WPA/WPA2 personal, AES-CCMP, WPI-SMS4, GCMP, WPS2.0, WAPI (hardware)
- Support of 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20 and 40 MHz Phased Coexistence Operation (PCO), unscheduled Power-Save Multi-Poll (PSMP)
- Support of 802.11w protected managed frames
- Support for 802.11ac STBC TX/RX, 4T1R beamformee, MU-MIMO RX, WoWLAN
- Support for MediaTek proprietary low power Green AP mode for portable hotspot operation
- Support of Wi-Fi Direct® (peer-to-peer wireless connection) and Wi-Fi Miracast® (Wi-Fi Display)
- Support of HotSpot 2.0 (HS2)
- Integrated 2.4 GHz PA with maximum 23 dBm CCK output power and 5 GHz PA with maximum 18.5 dBm OFDM 54 Mbps output power
- RX sensitivity at IEEE 802.11n HT20 MCS7 mode and -62 dBm at 5 GHz RX sensitivity at IEEE 802.11ac VHT80 MCS9 mode
- Support for 32 multicast address filters and TCP/UDP/IP checksum offload
- Support of per packet transmit power control
- QoS: WFA WMM, WMM PS

For more details, refer to MT6631 and MT7668 documentation.

3.13.3 Bluetooth (BT)

The BT module supports the following key features:

- Bluetooth 5 dual mode for LE 2 Mbps, LE long range, and advertise extension
- Integrated PA with 9 dBm (class 1) transmit power or 12 dBm boost mode via Wi-Fi PA.
- Receiver sensitivity:
  - GFSK: -95 dBm
  - DQPSK: -94.5 dBm
  - 8-DPSK: -88 dBm
  - BLE_1M: -98.5 dBm
  - BLE_2M: -95 dBm
  - BLE_500K: -101.5 dBm
  - BLE_125K: -104 dBm
- BT/Wi-Fi/LTE coexistence
- 7 BT links and 16 BLE links
- Packet Loss Concealment (PLC) function for better voice quality
- Wideband speech
- mSBC and SBC including mono and stereo
- Secure connection with AES-128 and ECC256
- Adaptive Frequency Hopping with built-in channel assessment method

For more details, refer to MT6631 and MT7668 documentation.

3.13.4 Global Navigation Satellite System (GNSS)

The GNSS module includes the following key features:

- Support for GPS/Glonass/Beidou/Galileo/QZSS tri-band reception concurrently
  - GPS/Galileo only (GPS only)
  - GPS/Galileo—GLONASS (G+G)
  - GPS/Beidou (G+B)
  - GPS/GLONASS/Beidou (G+G+B)
  - GPS/Galileo/GLONASS (G+G+G)
  - GPS/Galileo/GLONASS/Beidou (G+G+G+B)
- Support for Satellite-Based Augmentation Systems (SBAS): WAAS/MSAS/EGNOS/GAGAN
- Best-in-class sensitivity performance
  - -165 dBm tracking sensitivity
  - -163 dBm hot start sensitivity
  - -148 dBm cold start sensitivity
  - -151 dBm warm start sensitivity
- A-GPS sensitivity is 8 dB design margin over 3GPP
- Full A-GPS capability (EPO/HotStill)
- Active interference cancellation for up to 12 in-band tones
- Support for both Temperature-Compensated Crystal Oscillator (TCXO) and Thermistor Crystal (TMS) clock sources
- 5 Hz update rate

For more details, refer to MT6631 documentation.

3.13.5 FM System (FMSYS)

The FMSYS is an FM radio module, which includes the following key features:

- Broadcast band from 65 to 108 MHz with 50 kHz tune increment
- RDS/RBDS
- Digital stereo demodulator
- Simplified digital audio interface (I^2S)
- Stereo noise reduction
- Audio sensitivity 2 dBμVemf (SINAD = 26 dB)
- Audio SINAD 60 dB
- Anti-jamming
- Integrated short antenna

For more details, refer to MT6631 documentation.

3.13.6 Baseband Serial Interface (BSI)

The BSI is used to control external radio components. It transfers data to RF circuitry for PLL frequency change, reception gain setting, and other radio control purposes.

3.13.6.1 BSI Signal Descriptions

Table 3-49 presents BSI signal descriptions.

Table 3-49 BSI Signal Descriptions

Signal Name	Type	Description	Ball Location
RFIC			
RFIC_BSI_CK	DO	RFIC BSI clock	AF21
RFIC_BSI_D0	DIO	RFIC BSI data output 0	AF20
RFIC_BSI_D1	DIO	RFIC BSI data output 1	AE20
RFIC_BSI_D2	DIO	RFIC BSI data output 2	AG20
RFIC_BSI_EN	DO	RFIC BSI enable	AE21
SPM			
SPM_BSI_CK	DO	SPM BSI clock	AF21
SPM_BSI_D0	DO	SPM BSI data output 0	AF20
SPM_BSI_D1	DO	SPM BSI data output 1	AE20
SPM_BSI_D2	DO	SPM BSI data output 2	AG20
SPM_BSI_EN	DO	SPM BSI enable	AE21

3.13.7 Baseband Parallel Interface (BPI)

The BPI is used for connections to radio frequency circuits with strict time control, such as transmit permission, frequency band switching, etc.

3.13.7.1 BPI Signal Descriptions

Table 3-50 presents BPI signal descriptions.

Table 3-50 BPI Signal Descriptions

Signal Name	Type	Description	Ball Location
BPI_ANT0	DO	BPI_ANT0	AJ24
BPI_ANT1	DO	BPI_ANT1	AJ4
BPI_ANT2	DO	BPI_ANT2	AJ25
BPI_BUS0	DO	RF control bus bit 0	AC6
BPI_BUS1	DO	RF control bus bit 1	AH5
BPI_BUS2	DO	RF control bus bit 2	AG5
BPI_BUS3	DO	RF control bus bit 3	AF5
BPI_BUS4	DO	RF control bus bit 4	AE5
BPI_BUS5	DO	RF control bus bit 5	AD5
BPI_BUS6	DO	RF control bus bit 6	AJ5
BPI_BUS7	DO	RF control bus bit 7	AH6
BPI_BUS8	DO	RF control bus bit 8	AJ26
BPI_BUS9	DO	RF control bus bit 9	AH22
BPI_BUS10	DO	RF control bus bit 10	AJ22
BPI_OLAT0	DO	BPI control	AH4
BPI_OLAT1	DO	BPI control	AH26
BPI_OLAT2	DO	BPI control	AE6
BPI_OLAT3	DO	BPI control	AD6
BPI_PA_VM0	DO	BPI_PA_VM0	AH3
BPI_PA_VM1	DO	BPI_PA_VM1	AG4

3.13.8 Radio Frequency Front-End (RFFE) Interface

The MIPI RFFE℠ is a two-wire interface used for control of radio frequency front-end subsystems with strict performance requirements.

3.13.8.1 RFFE Signal Descriptions

Table 3-51 presents RFFE interface signal descriptions.

Table 3-51 RFFE Signal Descriptions

Signal Name	Type	Description	Ball Location
RFFE0			
MIPI0_SCLK	DO	RFFE0 interface clock	AJ7
MIPI0_SDATA	DIO	RFFE0 interface data	AJ8
RFFE1			
MIPI1_SCLK	DO	RFFE1 interface clock	AH7
MIPI1_SDATA	DIO	RFFE1 interface data	AG7
RFFE2			
MIPI2_SCLK	DO	RFFE2 interface clock	AF6
MIPI2_SDATA	DIO	RFFE2 interface data	AG6
RFFE3			
MIPI3_SCLK	DO	RFFE3 interface clock	AD6
MIPI3_SDATA	DIO	RFFE3 interface data	AE6
RFFE4			

Signal Name	Type	Description	Ball Location
MIPI4_SCLK	DO	RFFE4 interface clock	AH3
MIPI4_SDATA	DIO	RFFE4 interface data	AG4

3.14 Miscellaneous

3.14.1 Timers and Counters

3.14.1.1 System Timer (SYSTMR)

The SYSTMR is a 64-bit, always-on, up-counter which is used as a universal timer in the device. The counter value of SYSTMR is passed to A73, A53, SCP, GPU, and other processing units to provide uniform system timestamps for operating systems like Android™, Linux®, and RTOS.

The SYSTMR supports the following key features:

- Clocked by one of two available sources:
  - 26 MHz clock
  - 32 kHz clock
- Clock divider to allow the timer to tick with 26/13/6.5 MHz clock period (enabled by default for 13 MHz operation)
- HW counter incremented compensation when switching to 32 kHz clock source
- 12 x 32-bit counter timeout value (read as 32-bit down counter)
- Security access permission control for each control register (with one-time lock bit)

3.14.1.2 General-Purpose Timer (GPT)

The device has a GPT block (APXGPT) that supports the following features:

- 5 × 32-bit timers (GPT1 through GPT5)
- 1 × 64-bit timer (GPT6)
- Each GPT can operate on one of two selectable clock sources:
  - System clock (13 MHz)
  - RTC clock (32.768 kHz)
- Each GPT has a programmable clock division ratio (supported values: 1, 2, 3, 4 ...13, 16, 32, 64)
- Each GPT supports four operation modes: ONE-SHOT, REPEAT, KEEP-GO, FREERUN

3.14.1.3 Watchdog Timer (WDT)

The WDT module is a part of Top Reset Generation Unit (TOPRGU). For more information, refer to Section 5.5 Reset.

3.14.2 PMIC Wrapper (PWRAP)

The PWRAP serves as a bridge for the communication between CPU and PMIC.

The PWRAP supports the following key features:

- Fast auto SPI format generator for PMIC registers read/write
- APB3.0 bus lock scheme when SPI is busy
- Manual SPI format generator
- Dual I/O SPI mode
- Separated frequency between controller and SPI

3.14.2.1 PWRAP Signal Descriptions

Table 3-52 presents PWRAP signal descriptions.

Table 3-52 PWRAP Signal Descriptions

Signal Name	Type	Description	Ball Location
PWRAP SPI0			
PWRAP_SPI0_CK	DO	PWRAP serial clock	P23
PWRAP_SPI0_CSN	DO	PWRAP chip select	N23
PWRAP_SPI0_MI	DIO	PWRAP master input / slave output	P24, P25
PWRAP_SPI0_MO	DIO	PWRAP master output / slave input	P24, P25

3.14.3 Auxiliary Analog-to-Digital Converter (AUXADC)

The device features one AUXADC module. It is used to identify the plugged peripherals and perform temperature measurements.

The AUXADC module key features are:

- 12-bit Successive Approximation Register (SAR) ADC architecture
- 5 external and 2 internal channels operating in immediate mode
- Configurable auto-sampling function per channel
- Sequential channel serving from high to low channel
- Immediate analog-digital conversion with auto-set option
- Temperature measurement

3.14.3.1 AUXADC Signal Descriptions

Table 3-53 shows the AUXADC channels descriptions.

Table 3-53 AUXADC Signal Descriptions

Signal Name	Type	Description	Ball Location
AUXIN0[1][2]	AI	AUXADC external input channel 0	AF19
AUXIN1[1][2]	AI	AUXADC external input channel 1	AF18
AUXIN2[1][2]	AI	AUXADC external input channel 2	AE19
AUXIN3[1][2]	AI	AUXADC external input channel 3	AE18
AUXIN4[1][2]	AI	AUXADC external input channel 4	AG18
REFP[3]	AI	Positive reference voltage	AJ18

1. This pin should be connected to GND when unused.
2. All AUXIN* pins should be connected via a 0.1-µF capacitor to GND, as close as possible to the device, when used.
3. The REFP pin should be connected via a 1-µF capacitor to GND, as close as possible to the device, when used.

3.14.3.2 AUXADC Channel Mapping

Table 3-54 presents definitions of AUXADC channels.

Table 3-54 AUXADC Channel Mapping

AUXADC Channel ID	Description
Channel 0	External use (AUXIN0)
Channel 1	External use (AUXIN1)

AUXADC Channel ID	Description
Channel 2	External use (AUXIN2)
Channel 3	External use (AUXIN3)
Channel 4	External use (AUXIN4)
Channel 5	NA(1)
Channel 6	NA(1)
Channel 7	NA(1)
Channel 8	NA(1)
Channel 9	NA(1)
Channel 10	Internal use (TSENSE)
Channel 11	Internal use (TSENSE)
Channel 12	NA(1)
Channel 13	NA(1)
Channel 14	NA(1)
Channel 15	NA(1)

1. NA in this table = Not Applicable.

3.14.3.3 AUXADC Timing and Functional Characteristics

Table 3-55 presents timing and functional characteristics for auxiliary AUXADC interface in the device.

Table 3-55 AUXADC Specifications

Parameter		Min	Typ	Max	Unit
f_{OP}	Operating frequency		3.25		MHz
N	Resolution			12	bits
f_S	Sampling rate at N-bit		3.25 / (N+8)		MSPS
IN_{SW}	Input swing	0.05		1.45	V
C_{IN}	Input capacitance unselected channel		50		fF
	Input capacitance selected channel		4		pF
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Accuracy			±10	mV

3.14.4 Thermal Controller

The device thermal controller is based on several temperature sensors in the hot spots on the die. The thermal controller executes a periodic measurement for each hot spot. The temperature values are readable by software. In order to minimize the software effort to monitor temperature, the thermal controller generates interrupts to inform microprocessors of any abnormal condition.

The thermal controller supports the following key features:

- Up to four thermal sensors
- Periodic temperature measurement
- Temperature monitoring
- Different types of low pass filters for thermal sensor reading

Table 3-56 presents the Temperature Sensor (TSENSE) specifications.

Table 3-56 TSENSE Specifications

Parameter	Min	Typ	Max	Unit
Resolution		0.15		°C
Temperature range	0		85	°C
Accuracy		±5		°C

3.15 Boot Modes

The device supports the following boot modes:

- eMMC/UFS boot
- Boot ROM power down mode

The Boot ROM power down mode is used in the following scenarios:

- After system boot, boot ROM will be powered down and prevented from any probe of ROM content.
- In Multi-Core Deep Idle (MCDI), the Boot ROM is the bootstrap for suspend/resume CPU.

4 Ball Map

Figure 4-1 presents simplified diagram of the ball location on the package.

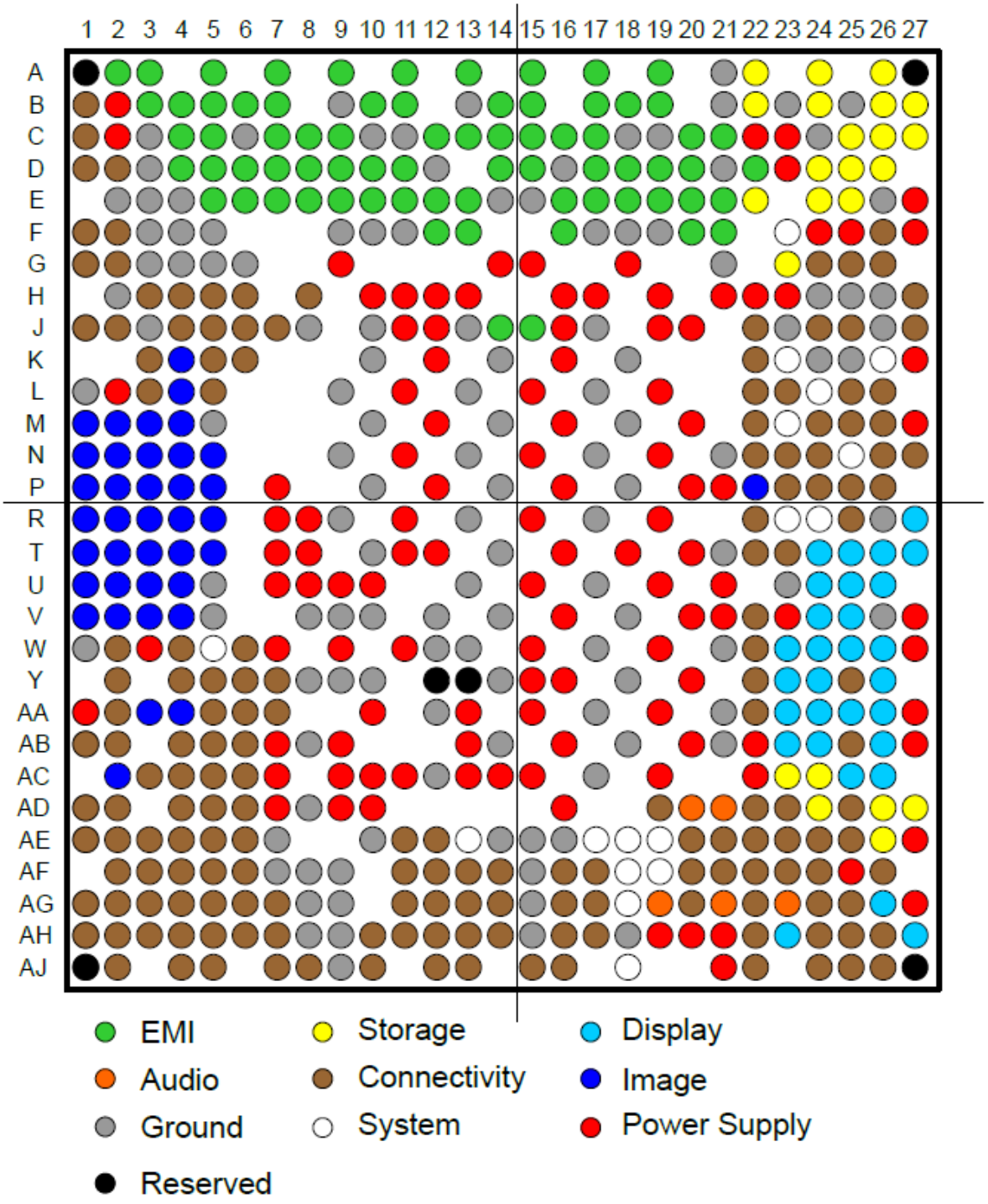


Figure 4-1 Ball Map Diagram

For detailed information about package outlines, thermal characteristics, and markings, see Section 7 Package Information.

4.1 Quadrant Pinout

Table 4-1 shows pin mapping on the top left part of the package.

Table 4-1 Ball Map-Top Left

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC_A1	EMI_EXTR	EMI0_DQ7		EMI0_DQ6		EMI0_CS1		EMI0_DQ11		EMI0_DQ12		EMI1_DQ10	
B	WF_IP	AVDD18_WBG	EMI0_DQ4	EMI0_DMI0	EMI0_CA2	EMI0_CA3	EMI0_CA4		DVSS	EMI0_DQ10	EMI0_DQ8		DVSS	EMI1_DQ14
C	WF_IN	AVDD12_WBG	DVSS	EMI0_DQS0_C	EMI0_DQ5	DVSS	EMI0_CA1	EMI0_DMI1	EMI0_DQ14	DVSS	DVSS	EMI1_DQ12	EMI1_DQ8	EMI1_DQ9
D	WF_QP	WF_QN	DVSS	EMI0_DQS0_T	EMI0_DQ1	EMI0_DQ3	EMI0_CKE1	EMI0_CS0	EMI0_DQ13	EMI0_CK_T	EMI0_DQ15	DVSS		EMI1_DQ15
E		DVSS	DVSS	DVSS	EMI0_DQ0	EMI0_DQ2	EMI0_CA5	EMI0_CKE0	EMI0_CA0	EMI0_CK_C	EMI0_DQ9	EMI0_DQS1_C	EMI1_DQS1_T	DVSS
F	BT_IN	BT_IP	DVSS	DVSS	DVSS				DVSS	DVSS	DVSS	EMI0_DQS1_T	EMI1_DQS1_C	
G	BT_QP	BT_QN	DVSS	DVSS	DVSS	DVSS			AVDD18_DDR					AVDDQ_EMI
H		DVSS	CONN_HRST_B	CONN_BT_CLK	CONN_BT_DATA	CONN_WF_CTRL2		XIN_WBG		AVDDQ_EMI	AVDD2_EMI	AVDDQ_EMI	AVDD2_EMI	
J	GPS_Q	GPS_I	DVSS	CONN_TOP_CLK	CONN_TOP_DATA	CONN_WF_CTRL0	CONN_WF_CTRL1	DVSS		DVSS	DVDD_CORE	DVDD_SRAM_CORE	DVSS	EMI_TN
K			CAM_RST3	CAM_CLK2	CAM_RST2	CONN_WB_PTA				DVSS		DVDD_CORE		DVSS
L	DVSS	DVDD18_IORT	CAM_PDN3	CAM_CLK3	CAM_PDN2				DVSS		DVDD_CORE		DVSS	
M	CSI1A_L0N	CSI1A_L0P	CSI1A_L1P	CSI1A_L1N	DVSS					DVSS		DVDD_CORE		DVSS
N	CSI1A_L2P	CSI1A_L2N	CSI1B_L0P	CSI1B_L0N	CSI0A_L2N_T1C				DVSS		DVDD_CORE		DVSS	
P	CSI1B_L1N	CSI1B_L1P	CSI0A_L0N_T0B	CSI0A_L0P_T0A	CSI0A_L2P_T1B		DVDD_CORE			DVSS		DVDD_CORE		DVSS

Table 4-2 shows pin mapping on the top right part of the package.

Table 4-2 Ball Map-Top Right

15	16	17	18	19	20	21	22	23	24	25	26	27	
EMI1_DQ13		EMI1_CA3		EMI1_DQ6		DVSS	UFS_RX0_RXP		UFS_TX0_N		MSDC0_DAT2	NC_A27	A
EMI1_DMI1		EMI1_CA2	EMI1_DMI0	EMI1_DQ5		DVSS	UFS_RX0_RXN	DVSS	UFS_TX0_P	DVSS	MSDC0_DAT0	MSDC0_DAT1	B
EMI1_CA1	EMI1_CS1	EMI1_CA4	DVSS	DVSS	EMI1_DQ4	EMI1_DQ7	AVDD09_UFS	AVDD12_UFS	DVSS	MSDC0_DAT5	MSDC0_DAT4	MSDC0_CMD	C
EMI1_DQ11	DVSS	EMI1_CA0	EMI1_CKE0	EMI1_CA5	EMI1_DQ2	DVSS	EMI_RESET_N	AVDD18_UFS	MSDC0_CLK	MSDC0_RSTB	MSDC0_DAT7		D
DVSS	EMI1_CK_T	EMI1_CS0	EMI1_CKE1	EMI1_DQ3	EMI1_DQ1	EMI1_DQS0_C	UFS_RST_N		MSDC0_DAT3	MSDC0_DSL	DVSS	DVDD18_MSDC0	E
	EMI1_CK_C	DVSS	DVSS	DVSS	EMI1_DQ0	EMI1_DQS0_T		UFS_CKIN_26M	DVDD_VQPS	AVDD33_USB	USB_DM	AVDD18_USB	F
AVDDQ_EMI			AVDD2_EMI			DVSS		MSDC0_DAT6	CHD_DM	CHD_DP	USB_DP		G
	AVDD2_EMI	AVDDQ_EMI		AVDDQ_EMI		DVDD_CORE	AVDD12_USB	AVDD18_SSUSB	DVSS	DVSS	DVSS	SSUSB_RXP	H
EMI_TP	DVDD_CORE	DVSS		DVDD_GPU	DVDD_GPU		AUD_DAT_MOSI0	DVSS	SSUSB_TXN	SSUSB_TXP	DVSS	SSUSB_RXN	J
	DVDD_CORE		DVSS				PERIPHERAL_EN8	SYSRSTB	DVSS	DVSS	RTC32K_CK	AVDD09_SSUSB	K
DVDD_CORE		DVSS		DVDD_GPU			PERIPHERAL_EN3	AUD_DAT_MISO1	TESTMODE	PERIPHERAL_EN1	AUD_SYNC_MOSI		L
	DVDD_CORE		DVSS		DVDD_GPU		PERIPHERAL_EN2	WATCHDOG	AUD_CLK_MOSI	AUD_CLK_MISO	AUD_SYNC_MISO	DVDD18_IOLT	M
DVDD_CORE		DVSS		DVDD_GPU		DVSS	PERIPHERAL_EN6	PWRAP_SPI0_CSN	AUD_DAT_MISO0	SCP_VREQ_VAO	SCL6	AUD_DAT_MOSI1	N
	DVDD_CORE		DVSS		DVDD_GPU	DVDD_CORE	ANT_SEL0	PWRAP_SPI0_CK	PWRAP_SPI0_MI	PWRAP_SPI0_MO	SDA6		P

Table 4-3 shows pin mapping on the bottom left part of the package.

Table 4-3 Ball Map-Bottom Left

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
R	CSI0A_L1N_T1A	CSI0A_L1P_T0C	CSI0B_L0P_T0A	CSI0B_L0N_T0B	CSI2A_L1N		DVDD_CORE	DVDD_CORE	DVSS		DVDD_CORE		DVSS	
T	CSI0B_L1N_T1A	CSI0B_L1P_T0C	CSI0B_L2P_T1B	CSI0B_L2N_T1C	CSI2A_L1P		DVDD_CORE	DVDD_CORE		DVSS	DVDD_SRAM_CORE	DVDD_CORE		DVSS
U	CSI2A_L0N	CSI2A_L0P	CSI2A_L2N	CSI2A_L2P	DVSS		DVDD_PROC_L	DVDD_PROC_L	DVDD_PROC_L	DVDD_PROC_L			DVSS	
V	CSI2B_L0N	CSI2B_L0P	CSI2B_L1N	CSI2B_L1P	DVSS			DVSS	DVSS	DVSS		DVSS		DVSS
W	DVSS	SDA4	AVDD12_CSI	EINT9	SRCLKENAI	CAM_PDN0	DVDD_SRAM_PROC_L		DVDD_PROC_L		DVDD_PROC_L	DVSS	DVSS	
Y		SCL4		EINT10	CAM_PDN1	PERIPHERAL_EN11	PERIPHERAL_EN10	DVSS	DVSS	DVSS		TN_PLLGP1	TP_PLLGP1	DVSS
AA	DVDD18_IORB	CAM_RST1	CAM_RST0	CAM_CLK0	KPROW0	PWM_A	PERIPHERAL_EN14			DVDD_PROC_B		DVSS	AVDD12_PLLGP	
AB	SDA2	SCL2		EINT1	EINT0	SCL0	DVDD_CORE	DVSS	DVDD_PROC_B				AVDD18_PLLGP	DVSS
AC		CAM_CLK1 CAM_CLK1	EINT4	KPCOL0	SDA0	BPI_BUS0	AVDD18_CPU		DVDD_PROC_B	DVDD_PROC_B	DVDD_PROC_B	DVSS	DVDD_SRAM_PROC_B	DVDD_SRAM_CORE
AD	UTXD0	URXD0		EINT8	BPI_BUS5	MISC_BSI_CK_3	DVDD_CORE	DVSS	DVDD_PROC_B	DVDD_PROC_B				
AE	EINT7	EINT6	KPCOL1	SCL1	BPI_BUS4	MISC_BSI_DO_3	CDM5P5A			DVSS	RFIC_ET0_P	RFIC_ET0_N	APC	DVSS
AF		EINT5	SPI_CLK	SDA1	BPI_BUS3	MISC_BSI_CK_2	CDM3P5A	DVSS	DVSS		TX_BB_IN1	TX_BB_QP1	TX_BB_IP0	TX_BB_QP0
AG	EINT3	EINT2	SPI_CSB	BPI_PA_VM1	BPI_BUS2	MISC_BSI_DO_2	MISC_BSI_DO_1	DVSS	DVSS		TX_BB_IP1	TX_BB_QN1	TX_BB_IN0	TX_BB_QN0
AH	KPROW1	SPI_MO	BPI_PA_VM0	BPI_OLAT0	BPI_BUS1	BPI_BUS7	MISC_BSI_CK_1	DVSS	DVSS	DET_QP1	DET_IN1	DET_IP1	DET_QN0	DET_QP0
AJ	NC_AJ1	SPI_MI		BPI_ANT1	BPI_BUS6		MISC_BSI_CK_0	MISC_BSI_DO_0	DVSS	DET_QN1		DET_IN0	DET_IP0	

Table 4-4 shows pin mapping on the bottom right part of the package.

Table 4-4 Ball Map-Bottom Right

15	16	17	18	19	20	21	22	23	24	25	26	27	
DVDD_CORE		DVSS		DVDD_GPU			ANT_SEL2	SRCLKENA0	SRCLKENA1	PERIPHERAL_EN0	DVSS	DSI0_D0N	R
	DVDD_CORE		DVDD_SRAM_GPU		DVDD_GPU	DVSS	PERIPHERAL_EN7	ANT_SEL1	DSI0_D3N	DSI0_D3P	DSI0_D1N	DSI0_D0P	T
DVDD_CORE		DVSS		DVDD_CORE		DVDD_CORE		DVSS	DSI0_CKN	DSI0_CKP	DSI0_D1P		U
	DVDD_CORE		DVSS		DVDD_CORE	DVDD_SRAM_CORE	PERIPHERAL_EN9	AVDD12_DSI	DSI0_D2N	DSI0_D2P	DVSS	AVDD04_DSI	V
DVDD_CORE		DVSS		DVDD_CORE		DVSS	SPI1_MI	DPI_D0	DPI_D6	DPI_D2	DPI_D3	DVDD18_IOLM	W
DVDD_SRAM_CORE	DVDD_CORE		DVSS		DVDD_CORE		SPI1_MO	DPI_HSYNC	DPI_D7	PERIPHERAL_EN4	DPI_D9		Y
DVDD_MODEM		DVSS		DVDD_MODEM		DVSS	SPI1_CLK	DPI_D11	DPI_VSYNC	DPI_D1	DPI_D10	DVDD18_MSDC1	AA
	DVDD_MODEM		DVSS		DVDD_MODEM	DVSS	DVDD_CORE	DPI_D5	DPI_D8	SPI1_CSB	DPI_D4	DVDD28_MSDC1	AB
DVDD_MODEM		DVSS		DVDD_MODEM			DVDD_CORE	MSDC1_DAT2	MSDC1_CLK	DPI_CK	DPI_DE		AC
	DVDD_MODEM			PERIPHERAL_EN13	I2S1_MCK	I2S1_LRCK	PERIPHERAL_EN12	SIM2_SCLK	MSDC1_DAT0	PERIPHERAL_EN5	MSDC1_CMD	MSDC1_DAT3	AD
DVSS	DVSS	MAIN_X26M_IN	AUXIN3	AUXIN2	RFIC0_BSI_D1	RFIC0_BSI_EN	SIM1_SRST	SIM1_SCLK	SIM2_SIO	SIM2_SRST	MSDC1_DAT1	DVDD28_SIM2	AE
DVSS	PRX_BB_I1	DRX_BB_Q1	AUXIN1	AUXIN0	RFIC0_BSI_D0	RFIC0_BSI_CK	SCL3	IDDIG	SIM1_SIO	DVDD28_SIM1	DRVBUS		AF
DVSS	PRX_BB_Q1	DRX_BB_I1	AUXIN4	I2S2_DI	RFIC0_BSI_D2	I2S1_DO	SDA3	I2S1_BCK	INT_SIM1	INT_SIM2	DSI_TE	DVDD18_SIM	AG
DVSS	DRX_BB_I0	DRX_BB_Q0	DVSS	AVDD18_MD	AVDD12_MD	AVDD18_AP	BPI_BUS9	DISP_PWM	SCL5	SDA5	BPI_OLAT1	LCM_RST	AH
PRX_BB_Q0	PRX_BB_I0		REFP			DVDD18_IOBL	BPI_BUS10		BPI_ANT0	BPI_ANT2	BPI_BUS8	NC_AJ27	AJ

4.2 Pin Characteristics

Table 4-5 describes the pin characteristics and the multiplexed signals on each ball.

Table 4-5 Pin Characteristics

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
EINT0	AB5	GPIO0	DIO	0	0	DVDD18	OFF	I
		PCM0_SYNC	DO	2				
		SRCLKENAI0	DI	4				
		SCP_SPI2_CS	DO	5				
		I2S3_MCK	DO	6				
		SPI2_CSB	DO	7				
EINT1	AB4	GPIO1	DIO	0	0	DVDD18	OFF	I
		PCM0_CLK	DO	2				
		CLKM3	DO	4				
		SCP_SPI2_MO	DO	5				
		I2S3_BCK	DO	6				
		SPI2_MO	DO	7				
EINT2	AG2	GPIO2	DIO	0	0	DVDD18	OFF	I
		PCM0_DO	DO	2				
		SCL6	DIO	4				
		SCP_SPI2_CK	DO	5				
		I2S3_LRCK	DO	6				
		SPI2_CLK	DO	7				
EINT3	AG1	GPIO3	DIO	0	0	DVDD18	OFF	I
		PCM0_DI	DI	2				
		SDA6	DIO	4				
		TDM_MCK	DO	5				
		I2S3_DO	DO	6				
		SCP_VREQ_VAO	DO	7				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
EINT4	AC3	GPIO4	DIO	0	0	DVDD18	OFF	I
		PWM_B	DO	1				
		I2S0_MCK	DO	2				
		TDM_BCK	DO	5				
EINT5	AF2	GPIO5	DIO	0	0	DVDD18	OFF	I
		PWM_C	DO	1				
		I2S0_BCK	DIO	2				
		TDM_LRCK	DO	5				
EINT6	AE2	GPIO6	DIO	0	0	DVDD18	OFF	I
		PWM_A	DO	1				
		I2S0_LRCK	DIO	2				
		IDDIG	DI	3				
		TDM_DATA0	DO	5				
		CMFLASH	DO	7				
EINT7	AE1	GPIO7	DIO	0	0	DVDD18	OFF	I
		SPI1_B_MI	DI	1				
		I2S0_DI	DI	2				
		USB_DRVVBUS	DO	3				
		TDM_DATA1	DO	5				
EINT8	AD4	GPIO8	DIO	0	0	DVDD18	OFF	I
		SPI1_B_CSB	DO	1				
		SCL7	DIO	3				
		TDM_DATA2	DO	5				
EINT9	W4	GPIO9	DIO	0	0	DVDD18	OFF	I
		SPI1_B_MO	DO	1				
		CMMCLK2	DO	3				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
EINT10	Y4	GPIO10	DIO	0	0	DVDD18	OFF	I
		SPI1_B_CLK	DO	1				
		CMMCLK3	DO	3				
		TDM_DATA3	DO	5				
SCL6	N26	GPIO11	DIO	0	0	DVDD18	OFF	I
		IDDIG	DI	2				
		SCL6	DIO	3				
		UCTS1	DI	4				
		UCTS0	DI	5				
		SRCLKENAI1	DI	6				
		I2S5_MCK	DO	7				
SDA6	P26	GPIO12	DIO	0	0	DVDD18	OFF	I
		USB_DRVVBUS	DO	2				
		SDA6	DIO	3				
		URTS1	DO	4				
		URTS0	DO	5				
		I2S2_DI2	DI	6				
		I2S5_BCK	DO	7				
DPI_D0	W23	GPIO13	DIO	0	0	DVDD18	OFF	I
		DBPI_D0	DIO	1				
		SPI5_MI	DI	2				
		PCM0_SYNC	DO	3				
		I2S0_MCK	DO	6				
DPI_D1	AA25	GPIO14	DIO	0	0	DVDD18	OFF	I
		DBPI_D1	DIO	1				
		SPI5_CSB	DO	2				
		PCM0_CLK	DO	3				
		I2S0_BCK	DIO	6				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
DPI_D2	W25	GPIO15	DIO	0	0	DVDD18	OFF	I
		DBPI_D2	DIO	1				
		SPI5_MO	DO	2				
		PCM0_DO	DO	3				
		I2S0_LRCK	DIO	6				
DPI_D3	W26	GPIO16	DIO	0	0	DVDD18	OFF	I
		DBPI_D3	DIO	1				
		SPI5_CLK	DO	2				
		PCM0_DI	DI	3				
		I2S0_DI	DI	6				
DPI_D4	AB26	GPIO17	DIO	0	0	DVDD18	OFF	I
		DBPI_D4	DIO	1				
		SPI4_MI	DI	2				
		I2S3_MCK	DO	6				
DPI_D5	AB23	GPIO18	DIO	0	0	DVDD18	OFF	I
		DBPI_D5	DIO	1				
		SPI4_CSB	DO	2				
		SCP_VREQ_VAO	DO	5				
		I2S3_BCK	DO	6				
DPI_D6	W24	GPIO19	DIO	0	0	DVDD18	OFF	I
		DBPI_D6	DIO	1				
		SPI4_MO	DO	2				
		URXD1	DI	5				
		I2S3_LRCK	DO	6				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
DPI_D7	Y24	GPIO20	DIO	0	0	DVDD18	OFF	I
		DBPI_D7	DIO	1				
		SPI4_CLK	DO	2				
		UTXD1	DO	5				
		I2S3_DO	DO	6				
DPI_D8	AB24	GPIO21	DIO	0	0	DVDD18	OFF	I
		DBPI_D8	DIO	1				
		SPI3_MI	DI	2				
		I2S2_MCK	DO	6				
DPI_D9	Y26	GPIO22	DIO	0	0	DVDD18	OFF	I
		DBPI_D9	DIO	1				
		SPI3_CSB	DO	2				
		I2S2_BCK	DO	6				
DPI_D10	AA26	GPIO23	DIO	0	0	DVDD18	OFF	I
		DBPI_D10	DIO	1				
		SPI3_MO	DO	2				
		UCTS1	DI	4				
		I2S2_LRCK	DO	6				
DPI_D11	AA23	GPIO24	DIO	0	0	DVDD18	OFF	I
		DBPI_D11	DIO	1				
		SPI3_CLK	DO	2				
		SRCLKENAI0	DI	3				
		URTS1	DO	4				
		I2S2_DI	DI	6				
DPI_HSYNC	Y23	GPIO25	DIO	0	0	DVDD18	OFF	I
		DBPI_HSYNC	DO	1				
		SCL6	DIO	3				
		KPCOL2	DIO	4				
		I2S1_MCK	DO	6				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
DPI_VSYNC	AA24	GPIO26	DIO	0	0	DVDD18	OFF	I
		DBPI_VSYNC	DO	1				
		SDA6	DIO	3				
		KPROW2	DIO	4				
		I2S1_BCK	DO	6				
DPI_DE	AC26	GPIO27	DIO	0	0	DVDD18	OFF	I
		DBPI_DE	DO	1				
		SCL7	DIO	3				
		DMIC_CLK	DO	4				
		I2S1_LRCK	DO	6				
DPI_CK	AC25	GPIO28	DIO	0	0	DVDD18	OFF	I
		DBPI_CK	DO	1				
		SDA7	DIO	3				
		DMIC_DAT	DI	4				
		I2S1_DO	DO	6				
MSDC1_CLK	AC24	GPIO29	DIO	0	1	DVDD28_MSDC1	OFF	OL
		MSDC1_CLK	DO	1				
		PCM1_CLK	DIO	6				
MSDC1_DAT3	AD27	GPIO30	DIO	0	1	DVDD28_MSDC1	PU	I
		MSDC1_DAT3	DIO	1				
		PCM1_DI	DI	6				
MSDC1_CMD	AD26	GPIO31	DIO	0	1	DVDD28_MSDC1	PU	I
		MSDC1_CMD	DIO	1				
		PCM1_SYNC	DIO	6				
MSDC1_DAT0	AD24	GPIO32	DIO	0	1	DVDD28_MSDC1	PU	I
		MSDC1_DAT0	DIO	1				
		PCM1_DO0	DO	6				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
MSDC1_DAT2	AC23	GPIO33	DIO	0	1	DVDD28_MSDC1	PU	I
		MSDC1_DAT2	DIO	1				
		PCM1_DO2	DO	6				
MSDC1_DAT1	AE26	GPIO34	DIO	0	1	DVDD28_MSDC1	PU	I
		MSDC1_DAT1	DIO	1				
		PCM1_DO1	DO	6				
SIM2_SIO	AE24	GPIO35	DIO	0	0	DVDD28_SIM2	OFF	I
SIM2_SRST	AE25	GPIO36	DIO	0	0	DVDD28_SIM2	OFF	I
SIM2_SCLK	AD23	GPIO37	DIO	0	0	DVDD28_SIM2	OFF	I
SIM1_SCLK	AE23	GPIO38	DIO	0	0	DVDD28_SIM1	OFF	I
SIM1_SRST	AE22	GPIO39	DIO	0	0	DVDD28_SIM1	OFF	I
SIM1_SIO	AF24	GPIO40	DIO	0	0	DVDD28_SIM1	OFF	I
IDDIG	AF23	GPIO41	DIO	0	0	DVDD18	OFF	I
		IDDIG	DI	1				
		URXD1	DI	2				
		UCTS0	DI	3				
		DMIC_CLK	DO	6				
DRVBUS	AF26	GPIO42	DIO	0	0	DVDD18	OFF	I
		USB_DRVVBUS	DO	1				
		UTXD1	DO	2				
		URTS0	DO	3				
		DMIC_DAT	DI	6				
DISP_PWM	AH23	GPIO43	DIO	0	0	DVDD18	OFF	I
		DISP_PWM	DO	1				
DSI_TE	AG26	GPIO44	DIO	0	0	DVDD18	OFF	I
		DSI_TE	DI	1				
LCM_RST	AH27	GPIO45	DIO	0	0	DVDD18	OFF	I
		LCM_RST	DO	1				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
INT_SIM2	AG25	GPIO46	DIO	0	0	DVDD18	OFF	I
		URXD1	DI	2				
		UCTS1	DI	3				
		IDDIG	DI	6				
		I2S5_LRCK	DO	7				
INT_SIM1	AG24	GPIO47	DIO	0	0	DVDD18	OFF	I
		UTXD1	DO	2				
		URTS1	DO	3				
		USB_DRVVBUS	DO	6				
		I2S5_DO	DO	7				
SCL5	AH24	GPIO48	DIO	0	1	DVDD18	PU	I
		SCL5	DIO	1				
SDA5	AH25	GPIO49	DIO	0	1	DVDD18	PU	I
		SDA5	DIO	1				
SCL3	AF22	GPIO50	DIO	0	1	DVDD18	PU	I
		SCL3	DIO	1				
SDA3	AG22	GPIO51	DIO	0	1	DVDD18	PU	I
		SDA3	DIO	1				
BPI_ANT2	AJ25	GPIO52	DIO	0	1	DVDD18	OFF	OL
		BPI_ANT2	DO	1				
BPI_ANT0	AJ24	GPIO53	DIO	0	1	DVDD18	OFF	OL
		BPI_ANT0	DO	1				
BPI_OLAT1	AH26	GPIO54	DIO	0	1	DVDD18	OFF	OL
		BPI_OLAT1	DO	1				
BPI_BUS8	AJ26	GPIO55	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS8	DO	1				
BPI_BUS9	AH22	GPIO56	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS9	DO	1				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
BPI_BUS10	AJ22	GPIO57	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS10	DO	1				
RFIC0_BSI_D2	AG20	GPIO58	DIO	0	1	DVDD18	OFF	I
		RFIC0_BSI_D2	DIO	1				
		SPM_BSI_D2	DO	2				
		PWM_B	DO	3				
RFIC0_BSI_D1	AE20	GPIO59	DIO	0	1	DVDD18	OFF	I
		RFIC0_BSI_D1	DIO	1				
		SPM_BSI_D1	DO	2				
RFIC0_BSI_D0	AF20	GPIO60	DIO	0	1	DVDD18	OFF	I
		RFIC0_BSI_D0	DIO	1				
		SPM_BSI_D0	DO	2				
MISC_BSI_DO_1	AG7	GPIO61	DIO	0	1	DVDD18	OFF	I
		MIPI1_SDATA	DIO	1				
MISC_BSI_CK_1	AH7	GPIO62	DIO	0	1	DVDD18	OFF	OL
		MIPI1_SCLK	DO	1				
MISC_BSI_DO_0	AJ8	GPIO63	DIO	0	1	DVDD18	OFF	I
		MIPI0_SDATA	DIO	1				
MISC_BSI_CK_0	AJ7	GPIO64	DIO	0	1	DVDD18	OFF	OL
		MIPI0_SCLK	DO	1				
MISC_BSI_DO_3	AE6	GPIO65	DIO	0	1	DVDD18	OFF	I
		MIPI3_SDATA	DIO	1				
		BPI_OLAT2	DO	2				
MISC_BSI_CK_3	AD6	GPIO66	DIO	0	1	DVDD18	OFF	OL
		MIPI3_SCLK	DO	1				
		BPI_OLAT3	DO	2				
MISC_BSI_DO_2	AG6	GPIO67	DIO	0	1	DVDD18	OFF	I
		MIPI2_SDATA	DIO	1				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
MISC_BSI_CK_2	AF6	GPIO68	DIO	0	1	DVDD18	OFF	OL
		MIPI2_SCLK	DO	1				
BPI_BUS7	AH6	GPIO69	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS7	DO	1				
BPI_BUS6	AJ5	GPIO70	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS6	DO	1				
BPI_BUS5	AD5	GPIO71	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS5	DO	1				
BPI_BUS4	AE5	GPIO72	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS4	DO	1				
BPI_BUS3	AF5	GPIO73	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS3	DO	1				
BPI_BUS2	AG5	GPIO74	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS2	DO	1				
BPI_BUS1	AH5	GPIO75	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS1	DO	1				
BPI_BUS0	AC6	GPIO76	DIO	0	1	DVDD18	OFF	OL
		BPI_BUS0	DO	1				
BPI_ANT1	AJ4	GPIO77	DIO	0	1	DVDD18	OFF	OL
		BPI_ANT1	DO	1				
BPI_OLAT0	AH4	GPIO78	DIO	0	1	DVDD18	OFF	OL
		BPI_OLAT0	DO	1				
BPI_PA_VM1	AG4	GPIO79	DIO	0	1	DVDD18	OFF	OL
		BPI_PA_VM1	DO	1				
		MIPI4_SDATA	DIO	2				
BPI_PA_VM0	AH3	GPIO80	DIO	0	1	DVDD18	OFF	OL
		BPI_PA_VM0	DO	1				
		MIPI4_SCLK	DO	2				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
SDA1	AF4	GPIO81	DIO	0	1	DVDD18	PU	I
		SDA1	DIO	1				
SDA0	AC5	GPIO82	DIO	0	1	DVDD18	PU	I
		SDA0	DIO	1				
SCL0	AB6	GPIO83	DIO	0	1	DVDD18	PU	I
		SCL0	DIO	1				
SCL1	AE4	GPIO84	DIO	0	1	DVDD18	PU	I
		SCL1	DIO	1				
SPI_MI	AJ2	GPIO85	DIO	0	0	DVDD18	OFF	I
		SPI0_MI	DI	1				
		SCP_SPI0_MI	DI	2				
		CLKM3	DO	3				
		I2S1_BCK	DO	4				
SPI_CSB	AG3	GPIO86	DIO	0	0	DVDD18	OFF	I
		SPI0_CSB	DO	1				
		SCP_SPI0_CS	DO	2				
		CLKM0	DO	3				
		I2S1_LRCK	DO	4				
SPI_MO	AH2	GPIO87	DIO	0	0	DVDD18	OFF	I
		SPI0_MO	DO	1				
		SCP_SPI0_MO	DO	2				
		SDA1	DIO	3				
		I2S1_DO	DO	4				
SPI_CLK	AF3	GPIO88	DIO	0	0	DVDD18	OFF	I
		SPI0_CLK	DO	1				
		SCP_SPI0_CK	DO	2				
		SCL1	DIO	3				
		I2S1_MCK	DO	4				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
SRCLKENAI	W5	GPIO89	DIO	0	0	DVDD18	OFF	I
		SRCLKENAI0	DI	1				
		PWM_C	DO	2				
		I2S5_BCK	DO	3				
		SDA8	DIO	5				
		CMVREF0	DO	6				
PWM_A	AA6	GPIO90	DIO	0	0	DVDD18	OFF	I
		PWM_A	DO	1				
		CMMCLK2	DO	2				
		I2S5_LRCK	DO	3				
		SCP_VREQ_VAO	DO	4				
		SCL8	DIO	5				
KPROW1	AH1	GPIO91	DIO	0	0	DVDD18	OFF	I
		KPROW1	DIO	1				
		PWM_B	DO	2				
		I2S5_DO	DO	3				
		CMMCLK3	DO	5				
KPROW0	AA5	GPIO92	DIO	0	1	DVDD18	OFF	OL
		KPROW0	DIO	1				
KPCOL0	AC4	GPIO93	DIO	0	1	DVDD18	PU	I
		KPCOL0	DIO	1				
KPCOL1	AE3	GPIO94	DIO	0	0	DVDD18	OFF	I
		KPCOL1	DIO	1				
		I2S2_DI2	DI	2				
		I2S5_MCK	DO	3				
		CMMCLK2	DO	4				
		SCP_SPI2_MI	DI	5				
		SRCLKENAI1	DI	6				
		SPI2_MI	DI	7				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
URXD0	AD2	GPIO95	DIO	0	1	DVDD18	PU	I
		URXD0	DI	1				
		UTXD0	DO	2				
UTXD0	AD1	GPIO96	DIO	0	1	DVDD18	PU	OH
		UTXD0	DO	1				
		URXD0	DI	2				
CAM_PDN0	W6	GPIO97	DIO	0	0	DVDD18	OFF	I
		UCTS0	DI	1				
		I2S2_MCK	DO	2				
		IDDIG	DI	3				
CAM_PDN1	Y5	GPIO98	DIO	0	0	DVDD18	OFF	I
		URTS0	DO	1				
		I2S2_BCK	DO	2				
		USB_DRVVBUS	DO	3				
CAM_CLK0	AA4	GPIO99	DIO	0	0	DVDD18	OFF	I
		CMMCLK0	DO	1				
CAM_CLK1	AC2	GPIO100	DIO	0	0	DVDD18	OFF	I
		CMMCLK1	DO	1				
		PWM_C	DO	2				
CAM_RST0	AA3	GPIO101	DIO	0	0	DVDD18	OFF	I
		CLKM2	DO	1				
		I2S2_LRCK	DO	2				
		CMVREF1	DO	3				
CAM_RST1	AA2	GPIO102	DIO	0	0	DVDD18	OFF	I
		CLKM1	DO	1				
		I2S2_DI	DI	2				
SCL2	AB2	GPIO103	DIO	0	1	DVDD18	PU	I
		SCL2	DIO	1				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
SDA2	AB1	GPIO104	DIO	0	1	DVDD18	PU	I
		SDA2	DIO	1				
SCL4	Y2	GPIO105	DIO	0	1	DVDD18	PU	I
		SCL4	DIO	1				
SDA4	W2	GPIO106	DIO	0	1	DVDD18	PU	I
		SDA4	DIO	1				
CAM_PDN2	L5	GPIO107	DIO	0	0	DVDD18	OFF	I
		DMIC_CLK	DO	1				
		CLKM0	DO	3				
		SDA7	DIO	4				
		PWM_A	DO	6				
CAM_CLK2	K4	GPIO108	DIO	0	0	DVDD18	OFF	I
		CMMCLK2	DO	1				
		CLKM1	DO	3				
		SCL8	DIO	4				
		PWM_B	DO	6				
CAM_RST2	K5	GPIO109	DIO	0	0	DVDD18	OFF	I
		DMIC_DAT	DI	1				
		CLKM2	DO	3				
		SDA8	DIO	4				
		PWM_C	DO	6				
CAM_PDN3	L3	GPIO110	DIO	0	0	DVDD18	OFF	I
		SCL7	DIO	1				
		USB_DRVVBUS	DO	4				
		SRCLKENAI1	DI	5				
		KPCOL2	DIO	6				
		URXD1	DI	7				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
CAM_CLK3	L4	GPIO111	DIO	0	0	DVDD18	OFF	I
		CMMCLK3	DO	1				
		SRCLKENAI0	DI	3				
		SCP_VREQ_VAO	DO	4				
CAM_RST3	K3	GPIO112	DIO	0	0	DVDD18	OFF	I
		SDA7	DIO	1				
		IDDIG	DI	4				
		AGPS_SYNC	DO	5				
		KPROW2	DIO	6				
		UTXD1	DO	7				
CONN_TOP_CLK	J4	GPIO113	DIO	0	0	DVDD18	OFF	I
		CONN_TOP_CLK	DO	1				
		SCL6	DIO	3				
CONN_TOP_DATA	J5	GPIO114	DIO	0	0	DVDD18	OFF	I
		CONN_TOP_DATA	DIO	1				
		SDA6	DIO	3				
CONN_BT_CLK	H4	GPIO115	DIO	0	0	DVDD18	OFF	I
		CONN_BT_CLK	DIO	1				
		UTXD1	DO	2				
CONN_BT_DATA	H5	GPIO116	DIO	0	0	DVDD18	OFF	I
		CONN_BT_DATA	DIO	1				
CONN_WF_CTRL0	J6	GPIO117	DIO	0	0	DVDD18	OFF	I
		CONN_WF_HB0	DIO	1				
CONN_WF_CTRL1	J7	GPIO118	DIO	0	0	DVDD18	OFF	I
		CONN_WF_HB1	DIO	1				
CONN_WF_CTRL2	H6	GPIO119	DIO	0	0	DVDD18	OFF	I
		CONN_WF_HB2	DIO	1				
CONN_WB_PTA	K6	GPIO120	DIO	0	0	DVDD18	OFF	I
		CONN_WB_PTA	DIO	1				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
CONN_HRST_B	H3	GPIO121	DIO	0	0	DVDD18	OFF	I
		CONN_HRST_B	DO	1				
		URXD1	DI	2				
MSDC0_CMD	C27	GPIO122	DIO	0	1	DVDD18_MSDC0	PU	I
		MSDC0_CMD	DIO	1				
MSDC0_DAT0	B26	GPIO123	DIO	0	1	DVDD18_MSDC0	PU	I
		MSDC0_DAT0	DIO	1				
MSDC0_CLK	D24	GPIO124	DIO	0	1	DVDD18_MSDC0	OFF	OL
		MSDC0_CLK	DO	1				
MSDC0_DAT2	A26	GPIO125	DIO	0	1	DVDD18_MSDC0	PU	I
		MSDC0_DAT2	DIO	1				
MSDC0_DAT4	C26	GPIO126	DIO	0	1	DVDD18_MSDC0	PU	I
		MSDC0_DAT4	DIO	1				
		UFS_MPHY_SCL	DI	6				
MSDC0_DAT6	G23	GPIO127	DIO	0	1	DVDD18_MSDC0	PU	I
		MSDC0_DAT6	DIO	1				
		UFS_MPHY_SDA	DIO	6				
MSDC0_DAT1	B27	GPIO128	DIO	0	1	DVDD18_MSDC0	PU	I
		MSDC0_DAT1	DIO	1				
		UFS_UNIPRO_SDA	DIO	6				
MSDC0_DAT5	C25	GPIO129	DIO	0	1	DVDD18_MSDC0	PU	I
		MSDC0_DAT5	DIO	1				
		UFS_UNIPRO_SCL	DI	6				
MSDC0_DAT7	D26	GPIO130	DIO	0	1	DVDD18_MSDC0	PU	I
		MSDC0_DAT7	DIO	1				
MSDC0_DSL	E25	GPIO131	DIO	0	1	DVDD18_MSDC0	OFF	I
		MSDC0_DSL	DI	1				
MSDC0_DAT3	E24	GPIO132	DIO	0	1	DVDD18_MSDC0	PU	I
		MSDC0_DAT3	DIO	1				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
MSDC0_RSTB	D25	GPIO133	DIO	0	1	DVDD18_MSDC0	PU	OH
		MSDC0_RSTB	DO	1				
		AGPS_SYNC	DO	3				
RTC32K_CK	K26	GPIO134	DIO	0	1	DVDD18	OFF	I
		RTC32K_CK	DI	1				
WATCHDOG	M23	GPIO135	DIO	0	1	DVDD18	OFF	OL
		WATCHDOG	DO	1				
AUD_CLK_MOSI	M24	GPIO136	DIO	0	0	DVDD18	OFF	I
		AUD_CLK_MOSI	DO	1				
		AUD_CLK_MISO	DI	2				
		I2S1_MCK	DO	3				
		UFS_UNIPRO_SCL	DI	6				
AUD_SYNC_MOSI	L26	GPIO137	DIO	0	0	DVDD18	OFF	I
		AUD_SYNC_MOSI	DO	1				
		AUD_SYNC_MISO	DI	2				
		I2S1_BCK	DO	3				
AUD_DAT_MOSI0	J22	GPIO138	DIO	0	0	DVDD18	OFF	I
		AUD_DAT_MOSI0	DO	1				
		AUD_DAT_MISO0	DI	2				
		I2S1_LRCK	DO	3				
AUD_DAT_MOSI1	N27	GPIO139	DIO	0	0	DVDD18	OFF	I
		AUD_DAT_MOSI1	DO	1				
		AUD_DAT_MISO1	DI	2				
		I2S1_DO	DO	3				
		UFS_MPHY_SDA	DIO	6				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
AUD_CLK_MISO	M25	GPIO140	DIO	0	0	DVDD18	OFF	I
		AUD_CLK_MISO	DI	1				
		AUD_CLK_MOSI	DO	2				
		I2S0_MCK	DO	3				
		UFS_UNIPRO_SDA	DIO	6				
AUD_SYNC_MISO	M26	GPIO141	DIO	0	0	DVDD18	OFF	I
		AUD_SYNC_MISO	DI	1				
		AUD_SYNC_MOSI	DO	2				
		I2S0_BCK	DO	3				
AUD_DAT_MISO0	N24	GPIO142	DIO	0	0	DVDD18	OFF	I
		AUD_DAT_MISO0	DI	1				
		AUD_DAT_MOSI0	DO	2				
		I2S0_LRCK	DO	3				
		VOW_DAT_MISO	DI	4				
AUD_DAT_MISO1	L23	GPIO143	DIO	0	0	DVDD18	OFF	I
		AUD_DAT_MISO1	DI	1				
		AUD_DAT_MOSI1	DO	2				
		I2S0_DI	DI	3				
		VOW_CLK_MISO	DI	4				
		UFS_MPHY_SCL	DI	6				
PWRAP_SPI0_MI	P24	GPIO144	DIO	0	1	DVDD18	OFF	I
		PWRAP_SPI0_MI	DIO	1				
		PWRAP_SPI0_MO	DIO	2				
PWRAP_SPI0_CSN	N23	GPIO145	DIO	0	1	DVDD18	PU	OH
		PWRAP_SPI0_CSN	DO	1				
PWRAP_SPI0_MO	P25	GPIO146	DIO	0	1	DVDD18	OFF	I
		PWRAP_SPI0_MO	DIO	1				
		PWRAP_SPI0_MI	DIO	2				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
PWRAP_SPI0_CK	P23	GPIO147	DIO	0	1	DVDD18	OFF	OL
		PWRAP_SPI0_CK	DO	1				
SRCLKENA0	R23	GPIO148	DIO	0	1	DVDD18	PU	OH
		SRCLKENA0	DO	1				
SRCLKENA1	R24	GPIO149	DIO	0	1	DVDD18	PU	OL
		SRCLKENA1	DO	1				
PERIPHERAL_EN0	R25	GPIO150	DIO	0	0	DVDD18	OFF	I
		PWM_A	DO	1				
		CMFLASH	DO	2				
		CLKM0	DO	3				
PERIPHERAL_EN1	L25	GPIO151	DIO	0	0	DVDD18	OFF	I
		PWM_B	DO	1				
		CMVREF0	DO	2				
		CLKM1	DO	3				
PERIPHERAL_EN2	M22	GPIO152	DIO	0	0	DVDD18	OFF	I
		PWM_C	DO	1				
		CMFLASH	DO	2				
		CLKM2	DO	3				
PERIPHERAL_EN3	L22	GPIO153	DIO	0	0	DVDD18	OFF	I
		PWM_A	DO	1				
		CMVREF0	DO	2				
		CLKM3	DO	3				
SCP_VREQ_VAO	N25	GPIO154	DIO	0	0	DVDD18	OFF	I
		SCP_VREQ_VAO	DO	1				
ANT_SEL0	P22	GPIO155	DIO	0	0	DVDD18	OFF	I
		CMVREF1	DO	3				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
ANT_SEL1	T23	GPIO156	DIO	0	0	DVDD18	OFF	I
		SRCLKENAI0	DI	2				
		SCL6	DIO	3				
		KPCOL2	DIO	4				
		IDDIG	DI	5				
ANT_SEL2	R22	GPIO157	DIO	0	0	DVDD18	OFF	I
		SRCLKENAI1	DI	2				
		SDA6	DIO	3				
		KPROW2	DIO	4				
		USB_DRVVBUS	DO	5				
PERIPHERAL_EN6	N22	GPIO158	DIO	0	0	DVDD18	OFF	I
PERIPHERAL_EN7	T22	GPIO159	DIO	0	0	DVDD18	OFF	I
PERIPHERAL_EN8	K22	GPIO160	DIO	0	0	DVDD18	OFF	I
SPI1_MI	W22	GPIO161	DIO	0	0	DVDD18	OFF	I
		SPI1_A_MI	DI	1				
		SCP_SPI1_MI	DI	2				
		IDDIG	DI	3				
		KPCOL2	DIO	5				
SPI1_CSB	AB25	GPIO162	DIO	0	0	DVDD18	OFF	I
		SPI1_A_CSB	DO	1				
		SCP_SPI1_CS	DO	2				
		USB_DRVVBUS	DO	3				
		KPROW2	DIO	5				
SPI1_MO	Y22	GPIO163	DIO	0	0	DVDD18	OFF	I
		SPI1_A_MO	DO	1				
		SCP_SPI1_MO	DO	2				
		SDA1	DIO	3				
		CMMCLK2	DO	5				
		DMIC_CLK	DO	6				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
SPI1_CLK	AA22	GPIO164	DIO	0	0	DVDD18	OFF	I
		SPI1_A_CLK	DO	1				
		SCP_SPI1_CK	DO	2				
		SCL1	DIO	3				
		CMMCLK3	DO	5				
		DMIC_DAT	DI	6				
PERIPHERAL_EN4	Y25	GPIO165	DIO	0	0	DVDD18	OFF	I
		PWM_B	DO	1				
		CMMCLK2	DO	2				
		SCP_VREQ_VAO	DO	3				
		TDM_MCK_2nd	DO	6				
PERIPHERAL_EN9	V22	GPIO166	DIO	0	0	DVDD18	OFF	I
RFIC0_BSI_EN	AE21	GPIO167	DIO	0	1	DVDD18	OFF	OL
		RFIC0_BSI_EN	DO	1				
		SPM_BSI_EN	DO	2				
RFIC0_BSI_CK	AF21	GPIO168	DIO	0	1	DVDD18	OFF	OL
		RFIC0_BSI_CK	DO	1				
		SPM_BSI_CK	DO	2				
PERIPHERAL_EN5	AD25	GPIO169	DIO	0	0	DVDD18	OFF	I
		PWM_C	DO	1				
		CMMCLK3	DO	2				
		CMVREF1	DO	3				
		AGPS_SYNC	DO	5				
		TDM_BCK_2nd	DO	6				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
I2S1_BCK	AG23	GPIO170	DIO	0	0	DVDD18	OFF	I
		I2S1_BCK	DO	1				
		I2S3_BCK	DO	2				
		SCL7	DIO	3				
		I2S5_BCK	DO	4				
		TDM_LRCK_2nd	DO	6				
I2S1_LRCK	AD21	GPIO171	DIO	0	0	DVDD18	OFF	I
		I2S1_LRCK	DO	1				
		I2S3_LRCK	DO	2				
		SDA7	DIO	3				
		I2S5_LRCK	DO	4				
		URXD1	DI	5				
		TDM_DATA0_2nd	DO	6				
I2S1_DO	AG21	GPIO172	DIO	0	0	DVDD18	OFF	I
		I2S1_DO	DO	1				
		I2S3_DO	DO	2				
		SCL8	DIO	3				
		I2S5_DO	DO	4				
		UTXD1	DO	5				
		TDM_DATA1_2nd	DO	6				
I2S1_MCK	AD20	GPIO173	DIO	0	0	DVDD18	OFF	I
		I2S1_MCK	DO	1				
		I2S3_MCK	DO	2				
		SDA8	DIO	3				
		I2S5_MCK	DO	4				
		UCTS0	DI	5				
		TDM_DATA2_2nd	DO	6				

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
I2S2_DI	AG19	GPIO174	DIO	0	0	DVDD18	OFF	I
		I2S2_DI	DI	1				
		I2S0_DI	DI	2				
		I2S2_DI2	DI	4				
		URTS0	DO	5				
		TDM_DATA3_2nd	DO	6				
PERIPHERAL_EN12	AD22	GPIO175	DIO	0	0	DVDD18	OFF	I
PERIPHERAL_EN13	AD19	GPIO176	DIO	0	0	DVDD18	OFF	I
PERIPHERAL_EN14	AA7	GPIO177	DIO	0	0	DVDD18	OFF	I
PERIPHERAL_EN10	Y7	GPIO178	DIO	0	0	DVDD18	OFF	I
PERIPHERAL_EN11	Y6	GPIO179	DIO	0	0	DVDD18	OFF	I
EMI0_DQ0	E5	EMI0_DQ0	DIO			AVDDQ_EMI		
EMI0_DQ1	D5	EMI0_DQ1	DIO			AVDDQ_EMI		
EMI0_DQ2	E6	EMI0_DQ2	DIO			AVDDQ_EMI		
EMI0_DQ3	D6	EMI0_DQ3	DIO			AVDDQ_EMI		
EMI0_DQ4	B3	EMI0_DQ4	DIO			AVDDQ_EMI		
EMI0_DQ5	C5	EMI0_DQ5	DIO			AVDDQ_EMI		
EMI0_DQ6	A5	EMI0_DQ6	DIO			AVDDQ_EMI		
EMI0_DQ7	A3	EMI0_DQ7	DIO			AVDDQ_EMI		
EMI0_DQ8	B11	EMI0_DQ8	DIO			AVDDQ_EMI		
EMI0_DQ9	E11	EMI0_DQ9	DIO			AVDDQ_EMI		
EMI0_DQ10	B10	EMI0_DQ10	DIO			AVDDQ_EMI		
EMI0_DQ11	A9	EMI0_DQ11	DIO			AVDDQ_EMI		
EMI0_DQ12	A11	EMI0_DQ12	DIO			AVDDQ_EMI		
EMI0_DQ13	D9	EMI0_DQ13	DIO			AVDDQ_EMI		
EMI0_DQ14	C9	EMI0_DQ14	DIO			AVDDQ_EMI		
EMI0_DQ15	D11	EMI0_DQ15	DIO			AVDDQ_EMI		
EMI0_DQS0_C	C4	EMI0_DQS0_C	DIO			AVDDQ_EMI		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
EMI0_DQS0_T	D4	EMI0_DQS0_T	DIO			AVDDQ_EMI		
EMI0_DQS1_C	E12	EMI0_DQS1_C	DIO			AVDDQ_EMI		
EMI0_DQS1_T	F12	EMI0_DQS1_T	DIO			AVDDQ_EMI		
EMI0_CA0	E9	EMI0_CA0	DIO			AVDDQ_EMI		
EMI0_CA1	C7	EMI0_CA1	DIO			AVDDQ_EMI		
EMI0_CA2	B5	EMI0_CA2	DIO			AVDDQ_EMI		
EMI0_CA3	B6	EMI0_CA3	DIO			AVDDQ_EMI		
EMI0_CA4	B7	EMI0_CA4	DIO			AVDDQ_EMI		
EMI0_CA5	E7	EMI0_CA5	DIO			AVDDQ_EMI		
EMI0_CS0	D8	EMI0_CS0	DIO			AVDDQ_EMI		
EMI0_CS1	A7	EMI0_CS1	DIO			AVDDQ_EMI		
EMI0_DMI0	B4	EMI0_DMI0	DIO			AVDDQ_EMI		
EMI0_DMI1	C8	EMI0_DMI1	DIO			AVDDQ_EMI		
EMI0_CKE0	E8	EMI0_CKE0	DIO			AVDDQ_EMI		
EMI0_CKE1	D7	EMI0_CKE1	DIO			AVDDQ_EMI		
EMI0_CK_C	E10	EMI0_CK_C	DIO			AVDDQ_EMI		
EMI0_CK_T	D10	EMI0_CK_T	DIO			AVDDQ_EMI		
EMI1_DQ0	F20	EMI1_DQ0	DIO			AVDDQ_EMI		
EMI1_DQ1	E20	EMI1_DQ1	DIO			AVDDQ_EMI		
EMI1_DQ2	D20	EMI1_DQ2	DIO			AVDDQ_EMI		
EMI1_DQ3	E19	EMI1_DQ3	DIO			AVDDQ_EMI		
EMI1_DQ4	C20	EMI1_DQ4	DIO			AVDDQ_EMI		
EMI1_DQ5	B19	EMI1_DQ5	DIO			AVDDQ_EMI		
EMI1_DQ6	A19	EMI1_DQ6	DIO			AVDDQ_EMI		
EMI1_DQ7	C21	EMI1_DQ7	DIO			AVDDQ_EMI		
EMI1_DQ8	C13	EMI1_DQ8	DIO			AVDDQ_EMI		
EMI1_DQ9	C14	EMI1_DQ9	DIO			AVDDQ_EMI		
EMI1_DQ10	A13	EMI1_DQ10	DIO			AVDDQ_EMI		
EMI1_DQ11	D15	EMI1_DQ11	DIO			AVDDQ_EMI		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
EMI1_DQ12	C12	EMI1_DQ12	DIO			AVDDQ_EMI		
EMI1_DQ13	A15	EMI1_DQ13	DIO			AVDDQ_EMI		
EMI1_DQ14	B14	EMI1_DQ14	DIO			AVDDQ_EMI		
EMI1_DQ15	D14	EMI1_DQ15	DIO			AVDDQ_EMI		
EMI1_DQS0_C	E21	EMI1_DQS0_C	DIO			AVDDQ_EMI		
EMI1_DQS0_T	F21	EMI1_DQS0_T	DIO			AVDDQ_EMI		
EMI1_DQS1_C	F13	EMI1_DQS1_C	DIO			AVDDQ_EMI		
EMI1_DQS1_T	E13	EMI1_DQS1_T	DIO			AVDDQ_EMI		
EMI1_CA0	D17	EMI1_CA0	DIO			AVDDQ_EMI		
EMI1_CA1	C15	EMI1_CA1	DIO			AVDDQ_EMI		
EMI1_CA2	B17	EMI1_CA2	DIO			AVDDQ_EMI		
EMI1_CA3	A17	EMI1_CA3	DIO			AVDDQ_EMI		
EMI1_CA4	C17	EMI1_CA4	DIO			AVDDQ_EMI		
EMI1_CA5	D19	EMI1_CA5	DIO			AVDDQ_EMI		
EMI1_CS0	E17	EMI1_CS0	DIO			AVDDQ_EMI		
EMI1_CS1	C16	EMI1_CS1	DIO			AVDDQ_EMI		
EMI1_DMI0	B18	EMI1_DMI0	DIO			AVDDQ_EMI		
EMI1_DMI1	B15	EMI1_DMI1	DIO			AVDDQ_EMI		
EMI1_CKE0	D18	EMI1_CKE0	DIO			AVDD2_EMI		
EMI1_CKE1	E18	EMI1_CKE1	DIO			AVDD2_EMI		
EMI1_CK_C	F16	EMI1_CK_C	DIO			AVDDQ_EMI		
EMI1_CK_T	E16	EMI1_CK_T	DIO			AVDDQ_EMI		
EMI_EXTR	A2	EMI_EXTR	DIO			AVDD2_EMI		
EMI_RESET_N	D22	EMI_RESET_N	DIO			AVDD2_EMI		
EMI_TP	J15	EMI_TP	DIO			AVDD2_EMI		
EMI_TN	J14	EMI_TN	DIO			AVDD18_DDR		
REFP	AJ18	REFP	AIO			AVDD18_MD		
AUXIN0	AF19	AUXIN0	AIO			AVDD18_MD		
AUXIN1	AF18	AUXIN1	AIO			AVDD18_MD		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
AUXIN2	AE19	AUXIN2	AIO			AVDD18_MD		
AUXIN3	AE18	AUXIN3	AIO			AVDD18_MD		
AUXIN4	AG18	AUXIN4	AIO			AVDD18_MD		
DET_IN0	AJ12	DET_IN0	AIO			AVDD18_MD		
DET_IP0	AJ13	DET_IP0	AIO			AVDD18_MD		
DET_QP0	AH14	DET_QP0	AIO			AVDD18_MD		
DET_QN0	AH13	DET_QN0	AIO			AVDD18_MD		
DET_IN1	AH11	DET_IN1	AIO			AVDD18_MD		
DET_IP1	AH12	DET_IP1	AIO			AVDD18_MD		
DET_QP1	AH10	DET_QP1	AIO			AVDD18_MD		
DET_QN1	AJ10	DET_QN1	AIO			AVDD18_MD		
TX_BB_QP0	AF14	TX_BB_QP0	AIO			AVDD18_MD		
TX_BB_QN0	AG14	TX_BB_QN0	AIO			AVDD18_MD		
TX_BB_IN0	AG13	TX_BB_IN0	AIO			AVDD18_MD		
TX_BB_IP0	AF13	TX_BB_IP0	AIO			AVDD18_MD		
TX_BB_QP1	AF12	TX_BB_QP1	AIO			AVDD18_MD		
TX_BB_QN1	AG12	TX_BB_QN1	AIO			AVDD18_MD		
TX_BB_IN1	AF11	TX_BB_IN1	AIO			AVDD18_MD		
TX_BB_IP1	AG11	TX_BB_IP1	AIO			AVDD18_MD		
MAIN_X26M_IN	AE17	MAIN_X26M_IN	AIO			AVDD18_MD		
PRX_BB_Q0	AJ15	PRX_BB_Q0	AIO			AVDD18_MD		
PRX_BB_I0	AJ16	PRX_BB_I0	AIO			AVDD18_MD		
DRX_BB_Q0	AH17	DRX_BB_Q0	AIO			AVDD18_MD		
DRX_BB_I0	AH16	DRX_BB_I0	AIO			AVDD18_MD		
PRX_BB_Q1	AG16	PRX_BB_Q1	AIO			AVDD18_MD		
PRX_BB_I1	AF16	PRX_BB_I1	AIO			AVDD18_MD		
DRX_BB_Q1	AF17	DRX_BB_Q1	AIO			AVDD18_MD		
DRX_BB_I1	AG17	DRX_BB_I1	AIO			AVDD18_MD		
RFIC_ET0_N	AE12	RFIC_ET0_N	AIO			AVDD18_MD		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
RFIC_ET0_P	AE11	RFIC_ET0_P	AIO			AVDD18_MD		
APC	AE13	APC	AIO			AVDD18_MD		
DSI0_CKN	U24	DSI0_CKN	AIO			AVDD12_DSI		
DSI0_CKP	U25	DSI0_CKP	AIO			AVDD12_DSI		
DSI0_D0N	R27	DSI0_D0N	AIO			AVDD12_DSI		
DSI0_D0P	T27	DSI0_D0P	AIO			AVDD12_DSI		
DSI0_D1N	T26	DSI0_D1N	AIO			AVDD12_DSI		
DSI0_D1P	U26	DSI0_D1P	AIO			AVDD12_DSI		
DSI0_D2N	V24	DSI0_D2N	AIO			AVDD12_DSI		
DSI0_D2P	V25	DSI0_D2P	AIO			AVDD12_DSI		
DSI0_D3N	T24	DSI0_D3N	AIO			AVDD12_DSI		
DSI0_D3P	T25	DSI0_D3P	AIO			AVDD12_DSI		
CSI0A_L0P_T0A	P4	CSI0A_L0P_T0A	AO			AVDD12_CSI		
CSI0A_L0N_T0B	P3	CSI0A_L0N_T0B	AIO			AVDD12_CSI		
CSI0A_L1P_T0C	R2	CSI0A_L1P_T0C	AIO			AVDD12_CSI		
CSI0A_L1N_T1A	R1	CSI0A_L1N_T1A	AIO			AVDD12_CSI		
CSI0A_L2P_T1B	P5	CSI0A_L2P_T1B	AIO			AVDD12_CSI		
CSI0A_L2N_T1C	N5	CSI0A_L2N_T1C	AIO			AVDD12_CSI		
CSI0B_L0P_T0A	R3	CSI0B_L0P_T0A	AIO			AVDD12_CSI		
CSI0B_L0N_T0B	R4	CSI0B_L0N_T0B	AIO			AVDD12_CSI		
CSI0B_L1P_T0C	T2	CSI0B_L1P_T0C	AIO			AVDD12_CSI		
CSI0B_L1N_T1A	T1	CSI0B_L1N_T1A	AIO			AVDD12_CSI		
CSI0B_L2P_T1B	T3	CSI0B_L2P_T1B	AIO			AVDD12_CSI		
CSI0B_L2N_T1C	T4	CSI0B_L2N_T1C	AIO			AVDD12_CSI		
CSI1A_L0P	M2	CSI1A_L0P	AIO			AVDD12_CSI		
CSI1A_L0N	M1	CSI1A_L0N	AIO			AVDD12_CSI		
CSI1A_L1P	M3	CSI1A_L1P	AIO			AVDD12_CSI		
CSI1A_L1N	M4	CSI1A_L1N	AIO			AVDD12_CSI		
CSI1A_L2P	N1	CSI1A_L2P	AIO			AVDD12_CSI		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
CSI1A_L2N	N2	CSI1A_L2N	AIO			AVDD12_CSI		
CSI1B_L0P	N3	CSI1B_L0P	AIO			AVDD12_CSI		
CSI1B_L0N	N4	CSI1B_L0N	AIO			AVDD12_CSI		
CSI1B_L1P	P2	CSI1B_L1P	AIO			AVDD12_CSI		
CSI1B_L1N	P1	CSI1B_L1N	AIO			AVDD12_CSI		
CSI2A_L0P	U2	CSI2A_L0P	AIO			AVDD12_CSI		
CSI2A_L0N	U1	CSI2A_L0N	AIO			AVDD12_CSI		
CSI2A_L1P	T5	CSI2A_L1P	AIO			AVDD12_CSI		
CSI2A_L1N	R5	CSI2A_L1N	AIO			AVDD12_CSI		
CSI2A_L2P	U4	CSI2A_L2P	AIO			AVDD12_CSI		
CSI2A_L2N	U3	CSI2A_L2N	AIO			AVDD12_CSI		
CSI2B_L0P	V2	CSI2B_L0P	AIO			AVDD12_CSI		
CSI2B_L0N	V1	CSI2B_L0N	AIO			AVDD12_CSI		
CSI2B_L1P	V4	CSI2B_L1P	AIO			AVDD12_CSI		
CSI2B_L1N	V3	CSI2B_L1N	AIO			AVDD12_CSI		
SSUSB_RXN	J27	SSUSB_RXN	AI			AVDD18_SSUSB		
SSUSB_RXP	H27	SSUSB_RXP	AI			AVDD18_SSUSB		
SSUSB_TXN	J24	SSUSB_TXN	AO			AVDD18_SSUSB		
SSUSB_TXP	J25	SSUSB_TXP	AO			AVDD18_SSUSB		
USB_DM	F26	USB_DM	AIO			AVDD33_USB		
USB_DP	G26	USB_DP	AIO			AVDD33_USB		
CHD_DM	G24	CHD_DM	AIO			AVDD33_USB		
CHD_DP	G25	CHD_DP	AIO			AVDD33_USB		
XIN_WBG	H8	XIN_WBG	AIO			AVDD18_WBG		
WF_IN	C1	WF_IN	AIO			AVDD18_WBG		
WF_IP	B1	WF_IP	AIO			AVDD18_WBG		
WF_QN	D2	WF_QN	AIO			AVDD18_WBG		
WF_QP	D1	WF_QP	AIO			AVDD18_WBG		
BT_IN	F1	BT_IN	AIO			AVDD18_WBG		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
BT_IP	F2	BT_IP	AIO			AVDD18_WBG		
BT_QN	G2	BT_QN	AIO			AVDD18_WBG		
BT_QP	G1	BT_QP	AIO			AVDD18_WBG		
GPS_I	J2	GPS_I	AIO			AVDD18_WBG		
GPS_Q	J1	GPS_Q	AIO			AVDD18_WBG		
UFS_CKIN_26M	F23	UFS_CKIN_26M	AIO			AVDD18_UFS		
UFS_TX0_P	B24	UFS_TX0_P	AIO			AVDD18_UFS		
UFS_TX0_N	A24	UFS_TX0_N	AIO			AVDD18_UFS		
UFS_RX0_RXP	A22	UFS_RX0_RXP	AIO			AVDD18_UFS		
UFS_RX0_RXN	B22	UFS_RX0_RXN	AIO			AVDD18_UFS		
UFS_RST_N	E22	UFS_RST_N	AIO			AVDD18_UFS		
AVDD04_DSI	V27	AVDD04_DSI	P					
AVDD09_SSUSB	K27	AVDD09_SSUSB	P					
AVDD09_UFS	C22	AVDD09_UFS	P					
AVDD12_CSI	W3	AVDD12_CSI	P					
AVDD12_DSI	V23	AVDD12_DSI	P					
AVDD12_MD	AH20	AVDD12_MD	P					
AVDD12_PLLGP	AA13	AVDD12_PLLGP	P					
AVDD12_UFS	C23	AVDD12_UFS	P					
AVDD12_USB	H22	AVDD12_USB	P					
AVDD12_WBG	C2	AVDD12_WBG	P					
AVDD18_AP	AH21	AVDD18_AP	P					
AVDD18_CPU	AC7	AVDD18_CPU	P					
AVDD18_DDR	G9	AVDD18_DDR	P					
AVDD18_MD	AH19	AVDD18_MD	P					
AVDD18_PLLGP	AB13	AVDD18_PLLGP	P					
AVDD18_SSUSB	H23	AVDD18_SSUSB	P					
AVDD18_UFS	D23	AVDD18_UFS	P					
AVDD18_USB	F27	AVDD04_DSI	P					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Power Domain	PU/PD Reset	IO Reset
AVDD18_WBG	B2	AVDD18_WBG	P					
AVDD2_EMI	G18	AVDD2_EMI	P					
AVDD33_USB	F25	AVDD33_USB	P					
AVDDQ_EMI	G14	AVDDQ_EMI	P					
DVDD_CORE	H21	DVDD_CORE	P					
DVDD_GPU	J19	DVDD_GPU	P					
DVDD_MODEM	AA15	DVDD_MODEM	P					
DVDD_PROC_B	AA10	DVDD_PROC_B	P					
DVDD_PROC_L	U7	DVDD_PROC_L	P					
DVDD_SRAM_CORE	J12	DVDD_SRAM_CORE	P					
DVDD_SRAM_GPU	T18	DVDD_SRAM_GPU	P					
DVDD_SRAM_PROC_B	AC13	DVDD_SRAM_PROC_B	P					
DVDD_SRAM_PROC_L	W7	DVDD_SRAM_PROC_L	P					
DVDD18_IOLT	M27	DVDD18_IOLT	P					
DVDD18_IOLM	W27	DVDD18_IOLM	P					
DVDD18_IOBL	AJ21	DVDD18_IOBL	P					
DVDD18_IORB	AA1	DVDD18_IORB	P					
DVDD18_IORT	L2	DVDD18_IORT	P					
DVDD18_MSDC0	E27	DVDD18_MSDC0	P					
DVDD18_MSDC1	AA27	DVDD18_MSDC1	P					
DVDD28_MSDC1	AB27	DVDD28_MSDC1	P					
DVDD18_SIM	AG27	DVDD18_SIM	P					
DVDD28_SIM1	AF25	DVDD28_SIM1	P					
DVDD28_SIM2	AE27	DVDD28_SIM2	P					
CDM3P5A	AF7	CDM3P5A	G					
CDM5P5A	AE7	CDM5P5A	G					
DVSS	A21	DVSS	G					
SYSRSTB	K23	SYSRSTB	DI					
TESTMODE	L24	TESTMODE	DI					

4.3 Power Rails

Table 4-6 lists the device power rails.

Table 4-6 Power Rails

Ball Name	Ball Location	Type	Description
AVDD04_DSI	V27	P	Analog power for DSI
AVDD09_SSUSB	K27	P	Analog power for SSUSB
AVDD09_UFS(1)	C22	P	Analog power for UFS
AVDD12_CSI	W3	P	Analog power for CSI
AVDD12_DSI	V23	P	Analog power for DSI
AVDD12_MD	AH20	P	Analog power for MODEM
AVDD12_PLLGP	AA13	P	Analog power for PLL
AVDD12_UFS	C23	P	Analog power for UFS
AVDD12_USB	H22	P	Analog power for USB
AVDD12_WBG	C2	P	Analog power for WBG (Wi-Fi, BT, GPS)
AVDD18_AP	AH21	P	Analog power input 1.8 V
AVDD18_CPU	AC7	P	Analog power input 1.8 V for A73/A53
AVDD18_DDR	G9	P	Analog power input 1.8 V for DRAM
AVDD18_MD	AH19	P	Analog power input 1.8 V for MODEM
AVDD18_PLLGP	AB13	P	Analog power input 1.8 V for PLL
AVDD18_SSUSB	H23	P	Analog power input 1.8 V for SSUSB
AVDD18_UFS	D23	P	Analog power 1.8 V for UFS
AVDD18_USB	F27	P	Analog power 1.8 V for USB
AVDD18_WBG	B2	P	Analog power 1.8 V for WBG
AVDD2_EMI	G18, H11, H13, H16	P	DRAM power
AVDD33_USB	F25	P	Analog power 3.3 V for USB
AVDDQ_EMI	G14, G15, H10, H12, H17, H19	P	DRAM power
DVDD_VQPS	F24	P	eFUSE blowing power control
DVDD_CORE	H21, J11, J16, K12, K16, L11, L15, M12, M16, N11, N15, P7, P12, P16, P21, R7, R8, R11, R15, T7, T8, T12, T16, U15, U19, U21, V16, V20, W15, W19, Y16, Y20, AB7, AB22, AC22, AD7	P	Digital power input for VPU
DVDD_GPU	J19, J20, L19, M20, N19, P20, R19, T20	P	Digital power input for GPU
DVDD_MODEM	AA15, AA19, AB16, AB20, AC15, AC19, AD16	P	Digital power input for LTE
DVDD_PROC_B	AA10, AB9, AC9, AC10, AC11, AD9, AD10	P	Digital power input for A73 core
DVDD_PROC_L	U7, U8, U9, U10, W9, W11	P	Digital power input for A53 core
DVDD_SRAM_CORE	J12, T11, V21, Y15, AC14	P	Digital power input for VPU SRAM

Ball Name	Ball Location	Type	Description
DVDD_SRAM_GPU	T18	P	Digital power input for GPU SRAM
DVDD_SRAM_PROC_B	AC13	P	Digital power input for A73 core SRAM
DVDD_SRAM_PROC_L	W7	P	Digital power input for A53 core SRAM
DVDD18_IOBL	AJ21	P	Digital power input for IO (region 3)
DVDD18_IOLM	W27	P	Digital power input for IO (region 2)
DVDD18_IOLT	M27	P	Digital power input for IO (region 1)
DVDD18_IORB	AA1	P	Digital power input for IO (region 4)
DVDD18_IORT	L2	P	Digital power input for IO (region 5)
DVDD18_MSDC0	E27	P	Digital power input for MSDC0
DVDD18_MSDC1	AA27	P	Digital power input for MSDC1
DVDD18_SIM	AG27	P	Digital power input for SIM1/2
DVDD28_MSDC1	AB27	P	Digital power input for MSDC1
DVDD28_SIM1	AF25	P	Digital power input for SIM1
DVDD28_SIM2	AE27	P	Digital power input for SIM2
CDM3P5A	AF7	G	Analog ground input for MODEM
CDM5P5A	AE7	G	Analog ground input for WBG
DVSS	A21, B9, B13, B21, B23, B25, C3, C6, C10, C11, C18, C19, C24, D3, D12, D16, D21, E2, E3, E4, E14, E15, E26, F3, F4, F5, F9, F10, F11, F17, F18, F19, G3, G4, G5, G6, G21, H2, H24, H25, H26, J3, J8, J10, J13, J17, J23, J26, K10, K14, K18, K24, K25, L1, L9, L13, L17, M5, M10, M14, M18, N9, N13, N17, N21, P10, P14, P18, R9, R13, R17, R26, T10, T14, T21, U5, U13, U17, U23, V5, V8, V9, V10, V12, V14, V18, V26, W1, W12, W13, W17, W21, Y8, Y9, Y10, Y14, Y18, AA12, AA17, AA21, AB8, AB14, AB18, AB21, AC12, AC17, AD8, AE10, AE14, AE15, AE16, AF8, AF9, AF15, AG8, AG9, AG15, AH8, AH9, AH15, AH18, AJ9	G	Digital ground

1. AVDD09_UFS must be connected to GND when UFS is not in use.

4.4 Reserved and Unused Pin Handling Recommendations

Table 4-7 provides specific ball handling recommendations for the case when the pins are not used.

Table 4-7 Reserved and Unused Pin Handling Recommendations

Ball Name	Requirement	Ball Location
TESTMODE	Test mode (tie to GND)	L24
NC_A1, NC_A27, NC_AJ1, NC_AJ27	NC, leave unconnected	A1, A27, AJ1, AJ27
AUD_CLK_MOSI, AUD_SYNC_MOSI, AUD_DAT_MOSI0, AUD_DAT_MOSI1, AUXIN0, AUXIN1, AUXIN2, AUXIN3, AUXIN4	These pins should be connected to GND when unused	M24, L26, J22, N27, AF19, AF18, AE19, AE18, AG18
TN_PLLGP1, TP_PLLGP1	Reserved, leave unconnected	Y12, Y13

NOTE:

- All other unused signal balls can be left floating.

5 Electrical Characteristics

Stresses above the values listed in Table 5-1 may cause permanent damage to the device. The recommended minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies based on characterization results. Exposure to absolute maximum rating conditions may affect device reliability.
The operating conditions in Table 5-2 must not be exceeded in order to ensure correct operation and reliability of the device. All parameters specified in this document refer to these operating conditions, unless noted otherwise.

5.1 Absolute Maximum Ratings

Table 5-1 represents the absolute maximum ratings of the device power pins.

Table 5-1 Absolute Maximum Ratings

Parameter		Conditions	Max	Unit
Digital power input for A73 core	DVDD_PROC_B, DVDD_SRAM_PROC_B		1.18	V
Digital power input for A53 core	DVDD_PROC_L, DVDD_SRAM_PROC_L		1.18	V
Digital power input for VPU	DVDD_CORE		0.84	V
Digital power input for GPU	DVDD_GPU		0.95	V
Analog power input	AVDD04_DSI		0.84	V
	AVDD09_SSUSB, AVDD09_UFS		0.99	V
	AVDD18_AP, AVDD18_CPU, AVDD18_DDR, AVDD18_MD, AVDD18_PLLGP, AVDD18_SSUSB, AVDD18_UFS, AVDD18_USB, AVDD18_WBG		1.98	V
	AVDD12_CSI, AVDD12_DSI, AVDD12_MD, AVDD12_PLLGP, AVDD12_UFS, AVDD12_USB, AVDD12_WBG		1.32	V
	AVDD2_EMI	LPDDR4/X	1.17	V
		LPDDR3	1.3	V
	AVDD33_USB		3.22	V
	AVDDQ_EMI	LPDDR4/X	0.63	V
		LPDDR3	1.3	V
Digital power input	DVDD18_IOLT, DVDD18_IOLM, DVDD18_IOBL, DVDD18_IORB, DVDD18_IORT		1.98	V
	DVDD18_MSDC0, DVDD18_MSDC1		1.95	V
	DVDD28_MSDC1, DVDD28_SIM1, DVDD28_SIM2		3.3	V
	DVDD_MODEM		0.79	V
	DVDD_SRAM_CORE		0.95	V
	DVDD_SRAM_GPU		1.05	V
Storage temperature			150	°C

5.1.1 Storage Conditions

Table 5-2 defines specifics for the storage conditions.

Table 5-2 Storage Conditions

Parameter		Min	Max	Unit
Shelf life in sealed bag	40 °C / 90% RH		24	months
After bag opened(1)				
Mounted	30 °C / 60% RH		168	h
Stored			20	% RH
Baking				
Low temperature device containers	40 °C +5 °C/-0 °C and < 5% RH	192		h
High temperature device containers	125 °C +5 °C/-0 °C	24		h

1. For devices subjected to infrared reflow, vapor-phase reflow, or equivalent processing.

5.2 Recommended Operating Conditions

Table 5-3 represents the recommended operating conditions of the device power pins.

Table 5-3 Recommended Operating Conditions

Pin Name	Description	Min	Typ	Max	Unit
AVDD04_DSI	Analog power for DSI	0.67	0.7	0.74	V
		0.76	0.8	0.84	V
AVDD09_SSUSB	Analog power for SSUSB	0.86	0.9	0.94	V
AVDD09_UFS	Analog power for UFS	0.86	0.9	0.94	V
AVDD12_CSI	Analog power for CSI	1.14	1.2	1.26	V
AVDD12_DSI	Analog power for DSI	1.14	1.2	1.26	V
AVDD12_MD	Analog power for MODEM	1.14	1.2	1.26	V
AVDD12_PLLGP	Analog power for PLLGP	1.14	1.2	1.26	V
AVDD12_UFS	Analog power for UFS	1.14	1.2	1.26	V
AVDD12_USB	Analog power for USB	1.14	1.2	1.26	V
AVDD12_WBG	Analog power for WBG	1.14	1.2	1.26	V
AVDD18_AP	Analog power for AP	1.71	1.8	1.89	V
AVDD18_CPU	Analog power for A73/A53	1.71	1.8	1.89	V
AVDD18_DDR	Analog power for DDR	1.71	1.8	1.89	V
AVDD18_MD	Analog power for MODEM	1.71	1.8	1.89	V
AVDD18_PLLGP	Analog power for PLLGP	1.71	1.8	1.89	V
AVDD18_SSUSB	Analog power for SSUSB	1.71	1.8	1.89	V
AVDD18_UFS	Analog power for UFS	1.71	1.8	1.89	V
AVDD18_USB	Analog power for USB	1.71	1.8	1.89	V
AVDD18_WBG	Analog power for WBG	1.71	1.8	1.89	V
AVDD33_USB	Analog power for USB	2.92	3.07	3.22	V
AVDD2_EMI	Analog power for LPDDR4/X	1.06	1.1	1.17	V
	Analog power for LPDDR3	1.14	1.2	1.3	V
AVDDQ_EMI	Analog power for LPDDR4/X	0.57	0.6	0.63	V
	Analog power for LPDDR3	1.14	1.2	1.3	V

Pin Name	Description	Min	Typ	Max	Unit
DVDD18_IOLT	Digital power input for 1.8 V IO	1.62	1.8	1.98	V
DVDD18_IOLM					
DVDD18_IOBL					
DVDD18_IORB					
DVDD18_IORT					
DVDD18_MSDC0	Digital power input for MSDC0	1.7	1.8	1.95	V
DVDD18_MSDC1	Digital power input for MSDC1	1.7	1.8	1.95	V
DVDD28_MC1	Digital power input for MSDC1	2.7	3	3.3	V
DVDD28_SIM1	Digital power input for SIM1	2.7	3	3.3	V
DVDD28_SIM2	Digital power input for SIM2	2.7	3	3.3	V
DVDD_CORE	Digital power input for VPU (0.6 V is only for IDLE state)	0.57	0.6	0.63	V
		0.67	0.7	0.74	V
		0.76	0.8	0.84	V
DVDD_GPU	Digital power input for GPU	0.57	0.6	0.63	V
		0.67	0.7	0.74	V
		0.76	0.8	0.84	V
		0.86	0.9	0.95	V
DVDD_PROC_B	Digital power input for A73	0.57	0.6	0.63	V
		0.67	0.7	0.74	V
		0.76	0.8	0.84	V
		0.9	0.95	1	V
		1.06	1.12	1.18	V
DVDD_PROC_L	Digital power input for A53	0.57	0.6	0.63	V
		0.67	0.7	0.74	V
		0.76	0.8	0.84	V
		0.9	0.95	1	V
		1.06	1.12	1.18	V
DVDD_MODEM	Digital power input for MODEM (0.55 V is only for IDLE state)	0.52	0.55	0.58	V
		0.62	0.65	0.68	V
		0.67	0.7	0.74	V
		0.71	0.75	0.79	V
DVDD_SRAM_CORE	Digital power input for VPU SRAM (0.6 V is only for IDLE state)	0.57	0.6	0.63	V
		0.86	0.9	0.95	V
DVDD_SRAM_GPU	Digital power input for GPU	0.81	0.85	0.89	V
		0.86	0.9	0.95	V
		0.95	1	1.05	V
DVDD_SRAM_PROC_B	Digital power input for A73 SRAM	0.86	0.9	0.95	V
		1	1.05	1.1	V
		1.06	1.12	1.18	V
DVDD_SRAM_PROC_L	Digital power input for A53 SRAM	0.86	0.9	0.95	V
		1	1.05	1.1	V
		1.06	1.12	1.18	V
Operating junction temperature		-20		125	°C

5.3 DC Electrical Specifications

This section provides DC electrical characteristics per buffer type.

5.3.1 RTCIO DC Specifications

Table 5-4 shows RTCIO DC buffer electrical characteristics.

Table 5-4 RTCIO DC Specifications

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic low voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic high voltage	-0.3		0.35 × VDDIO(1)	V
F_{RTC}	Input clock frequency		32		kHz
DC_{RTC}	Input signal duty cycle	45	50	55	%
OUTPUT					
V_{OH}	DC output logic low voltage	0.75 × VDDIO(1)			V
V_{OL}	DC output logic high voltage			0.25 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IOLT). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.2 SPII2SIO DC Specifications

Table 5-5 shows SPII2SIO DC buffer electrical characteristics.

Table 5-5 SPII2SIO DC Specifications

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic low voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic high voltage	-0.3		0.35 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic low voltage	0.75 × VDDIO(1)			V
V_{OL}	DC Output logic high voltage			0.25 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IORB). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.3 I2C012IO DC Specifications

Table 5-6 shows I2C012IO DC buffer electrical characteristics.

Table 5-6 I2C012IO DC Specifications

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic low voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic high voltage	-0.3		0.35 × VDDIO(1)	V
OUTPUT					
V_{OL}	DC output logic high voltage			0.2 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IORB). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.4 I2C3IO DC Specifications

Table 5-7 shows I2C3IO DC buffer specifications.

Table 5-7 I2C3IO DC Specifications

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic low voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic high voltage	-0.3		0.35 × VDDIO(1)	V
OUTPUT					
V_{OL}	DC output logic high voltage			0.2 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IOLB). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.5 MSDC0IO DC Specifications

Table 5-8 shows MSDC0IO DC buffer specifications.

Table 5-8 MSDC0IO DC Specifications

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic low voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic high voltage	-0.3		0.35 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic low voltage	1.4			V
V_{OL}	DC output logic high voltage			0.45	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_MSDC0). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.6 MSDC1IO DC Specifications

Table 5-9 shows MSDC1IO DC buffer specifications.

Table 5-9 MSDC1IO DC Specifications (2.8 V/3.3 V)

Parameters		Min	Typ	Max	Unit
Operating voltage = 2.8 V/3.3 V					
INPUT					
V_{IH}	Input logic low voltage	0.625 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic high voltage	-0.3		0.25 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic low voltage	0.75 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{OL}	DC output logic high voltage	-0.3		0.125 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD28_MSDC1). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

Table 5-10 MSDC1IO DC Specifications (1.8 V)

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic low voltage	1.27		VDDIO(1) + 0.3	V
V_{IL}	Input logic high voltage	-0.3		0.58	V
OUTPUT					
V_{OH}	DC output logic low voltage	1.4		VDDIO(1) + 0.3	V
V_{OL}	DC output logic high voltage	-0.3		0.45	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_MSDC1). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.7 DDRIO DC Specifications

The EMI LPDDR3 electrical characteristics are compliant with JEDEC Standard—JESD209-3C.

The EMI LPDDR4 electrical characteristics are compliant with JEDEC Standard—JESD209-4B.

5.4 Power Management

5.4.1 Power Sequences

Refer to MT6358 PMIC datasheet for detailed timing sequence.

5.5 Reset

Top Reset Generation Unit (TOPRGU) generates reset signals and distributes them to each system. A WDT is also included in this module.

The TOPRGU supports the following features:

- Hardware reset signals for the whole chip
- Software controllable reset
- WDT
- Reset output signals for companion chips

Figure 5-1 shows the block diagram of TOPRGU in the MT8385.

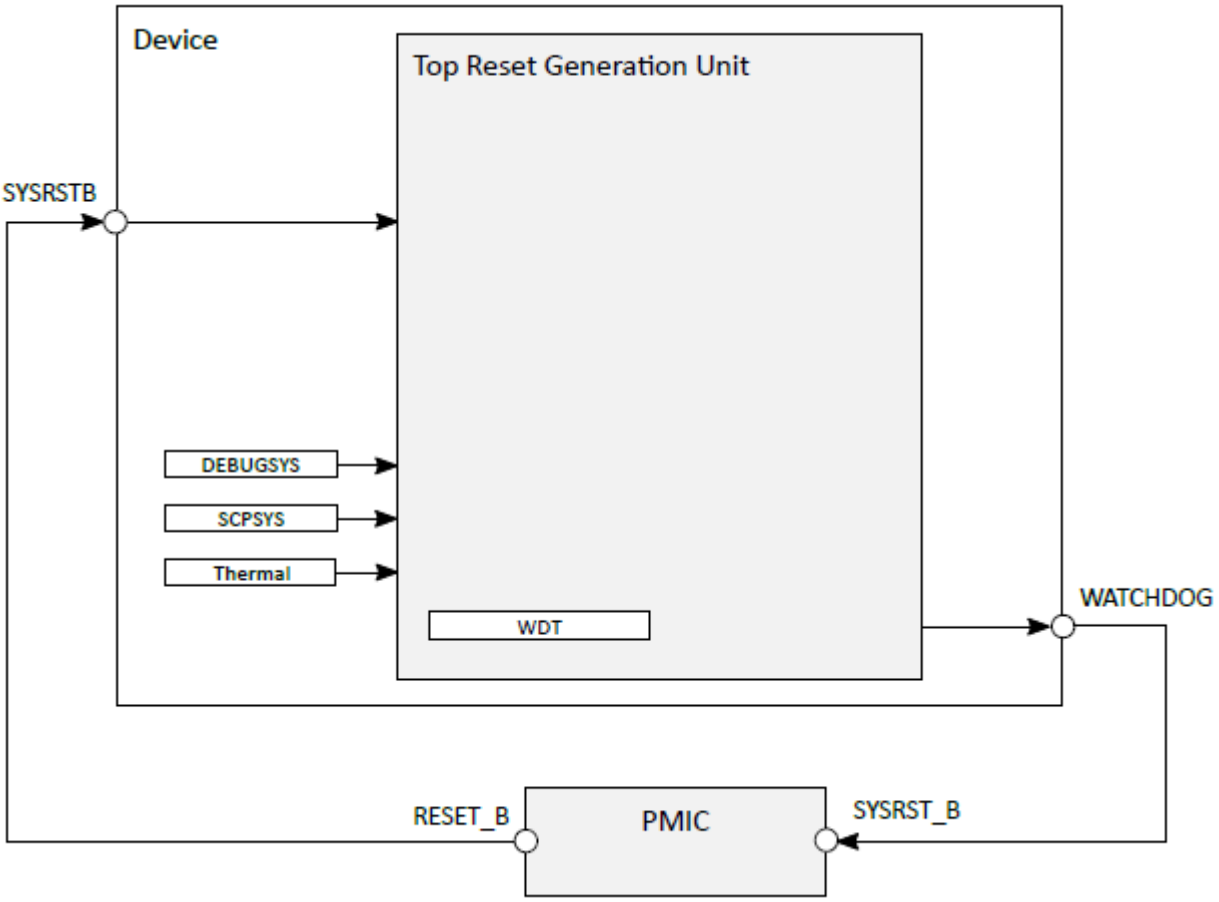


Figure 5-1 Reset Block Diagram

5.5.1 Reset Signal Descriptions

Table 5-11 shows Reset signal description.

Table 5-11 Reset Signal Descriptions

Signal Name	Type	Description	Ball Location
SYSRSTB	DI	System reset input	K23
WATCHDOG	DO	Watchdog reset output	M23

5.5.2 Reset Timing Characteristics

Table 5-12 presents timing characteristics for Resets in the device.

Table 5-12 Reset Timing Characteristics

Min	Parameter	
RST01	t_w	Pulse width, RESET
RST02	t_h	Hold time, RESET after all supplies valid

6 Clock Characteristics

The device has four external input clocks— low frequency (RTC32K_CK), high frequency (MAIN_X26M_IN), wireless (XIN_WBG), and UFS (UFS_CKIN_26M).

Figure 6-1 shows the external clock sources and clock outputs.

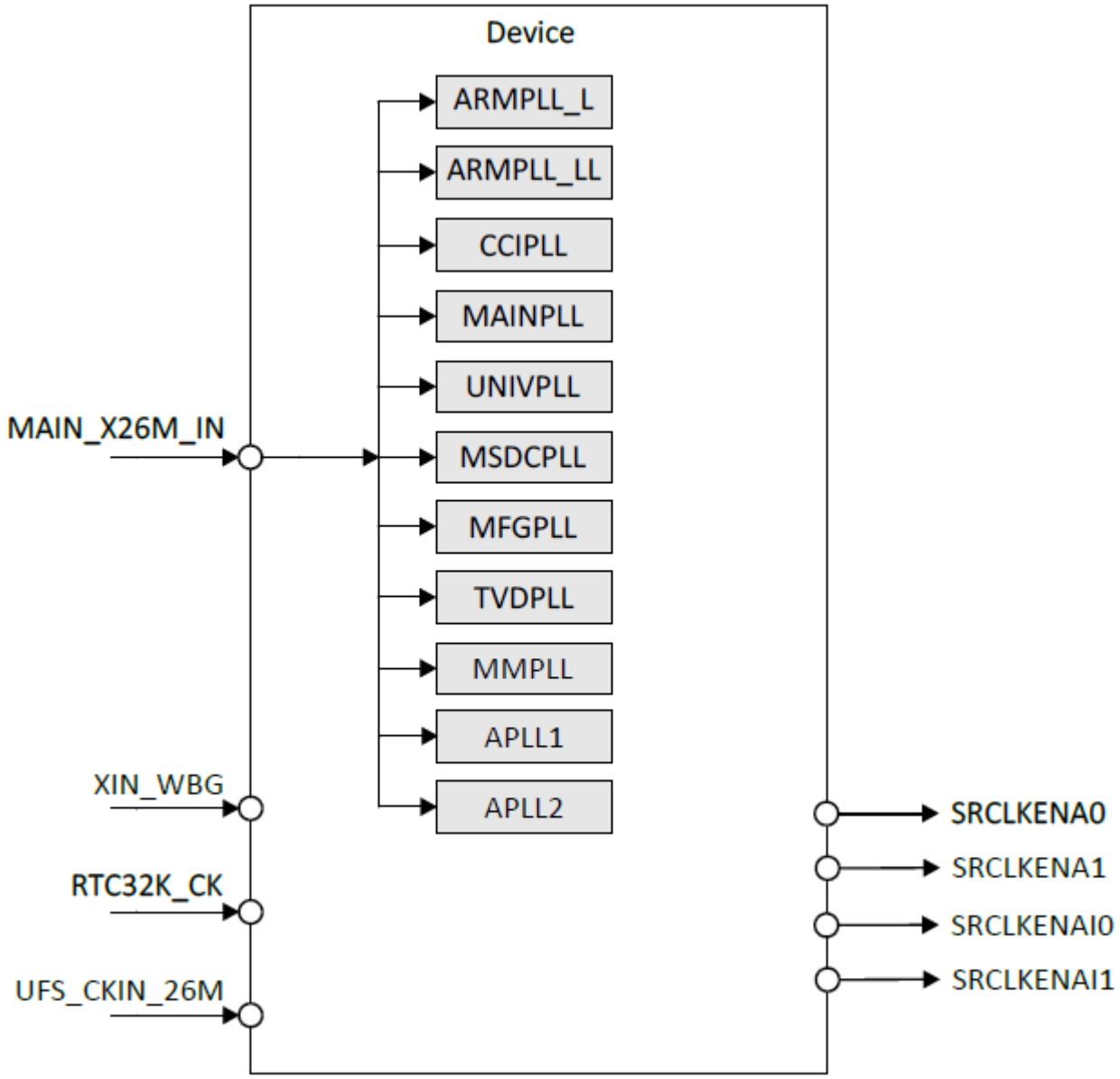


Figure 6-1 Device Clock Diagram

6.1 Maximum Performance Ratings

Table 6-1 shows the maximum core and peripheral performance limitations and correlations.

Table 6-1 Maximum Performance Ratings

Module		Max	Unit
Quad-core Arm Cortex-A73	A73	2000	MHz
Quad-core Arm Cortex-A53	A53	2000	MHz

Module		Max	Unit
Graphics Accelerator Mali G-72 MP3	GPU	800	MHz
System Companion Processor	SCP	416	MHz
Vision Processing Unit VP6 DSP	VPU	525	MHz
External Memory Interface	LPDDR3	1866	MHz
	LPDDR4/X	3733	MHz
Memory Card Controller	eMMC	200	MHz
	SD Card/SDIO	200	MHz
Universal Flash Storage	UFS	5830.4	Mbps
Display Parallel Interface	DPI	148.5	MHz
Display Serial Interface	DSI	1.5	Gbps/Lane
Image Signal Processor	ISP	32	MPix@30fps
Camera Serial Interface	CSI D-PHY	2.8	Gbps/Lane
	CSI C-PHY	2.5	Gbps/Lane
Video Encoder	VENC	1920 × 1080	Pix@30fps
Video Decoder	VDEC	1920 × 1080	Pix@30fps
Inter-IC Sound	I2S master mode (sampling frequency)	192	kHz
	I2S slave mode (sampling frequency)	48	kHz
Pulse Code Modulation	PCM (sampling frequency)	48	kHz
Pulse Density Modulation	PDM (clock)	3.25	MHz
Time Division Multiplexed Interface	TDM (TX sampling frequency)	192	kHz
Inter-Integrated Circuit	I2C (HS mode)	3.4	Mbps
Universal Asynchronous Receiver/Transmitter	UART	961,200	bps
Serial Peripheral Interface	SPI	54.945	MHz
SuperSpeed Universal Serial Bus	SSUSB SuperSpeed	5	Gbps
	SSUSB High-Speed	480	Mbps
	SSUSB Full-Speed	12	Mbps
	SSUSB Low-Speed	1.5	Mbps
Pulse Width Modulation	PWM	13	MHz
Auxiliary ADC	AUXADC (clock rate)	3.25	MHz

6.2 PLL Specifications

Table 6-2 shows ARMPLL_L specifications.

Table 6-2 ARMPLL_L Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		2000		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-3 shows ARMPLL_LL specifications.

Table 6-3 ARMPLL_LL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		800		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-4 shows MAINPLL specifications.

Table 6-4 MAINPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		1092		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			30	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-5 shows MFGPLL specifications.

Table 6-5 MFGPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		520		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-6 shows MMPLL specifications.

Table 6-6 MMPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		420		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-7 shows UNIVPLL specifications.

Table 6-7 UNIVPLL Specifications

Parameter		Mode	Min	Typ	Max	Unit
F_{IN}	Input clock frequency			26		MHz
F_{OUT}	Output clock frequency	PLL		2496		MHz
		USB		192		MHz
t_{SET}	Settling time			20		µs
$F_{OUT(D)}$	Output clock duty cycle		47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)	1248 MHz			30	ps
		192 MHz			60	ps
DVDD	Digital power supply		0.54	0.8	0.88	V
AVDD18	Analog power supply		1.71	1.8	1.89	V
AVDD12	Analog power supply		1.14	1.2	1.26	V

Table 6-8 shows MSDCPLL specifications.

Table 6-8 MSDCPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		416		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-9 shows APLL1 specifications.

Table 6-9 APLL1 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		180.6336		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-10 shows APLL2 specifications.

Table 6-10 APLL2 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.608		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps

Parameter		Min	Typ	Max	Unit
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-11 shows CCIPLL specifications.

Table 6-11 CCIPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		800		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-12 shows TVDPLL specifications.

Table 6-12 TVDPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		594		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

6.3 Clock Squarer

For digital circuits to work well, most VCXO have a sinusoidal waveform output clock with too small amplitude (about several hundred mV). The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

Table 6-13 shows the specifications of the clock squarer.

Table 6-13 Clock Squarer Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency	13	26		MHz
V_{IN}	Input signal amplitude	400	800	1200	mVpp
	Maximum Positive Overshoot			1.32	V
	Minimum Negative Overshoot	-0.1			V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C

6.4 Clock Signal Descriptions

Table 6-14 presents clock signal descriptions.

Table 6-14 Clock Signal Descriptions

Signal Name	Type	Description	Ball Location
MAIN_X26M_IN	AIO	26 MHz clock input	AE17
UFS_CKIN_26M	AIO	26 MHz clock input for UFS	F23
RTC32K_CK	DI	RTC 32 kHz clock input	K26
XIN_WBG	AIO	WBG crystal clock input	H8
SRCLKENA0	DO	Output signal; control of PMIC 26 MHz / Buck / LDO	R23
		Normal mode or sleep mode: • High: Normal mode • Low: Sleep mode or low power mode	
SRCLKENA1	DO	Output signal; control of PMIC 26 MHz / Buck / LDO on or off	R24
SRCLKENAI0	DI	SRCLKENA0 invert	AB5, AA23, W5, L4, T23
SRCLKENAI1	DI	SRCLKENA1 invert	N26, AE3, L3, R22

7 Package Information

7.1 Thermal Specifications

7.1.1 Thermal Operating Specifications

Table 7-1 presents the thermal resistance characteristics and maximum operating temperatures of the device.

Table 7-1 Thermal Operating Specifications

Parameter		Value	Unit
θ_{JA}	Package thermal resistances in nature convection	37.65	°C/Watt

7.2 Top Marking

Figure 7-1 shows the device top marking definition.

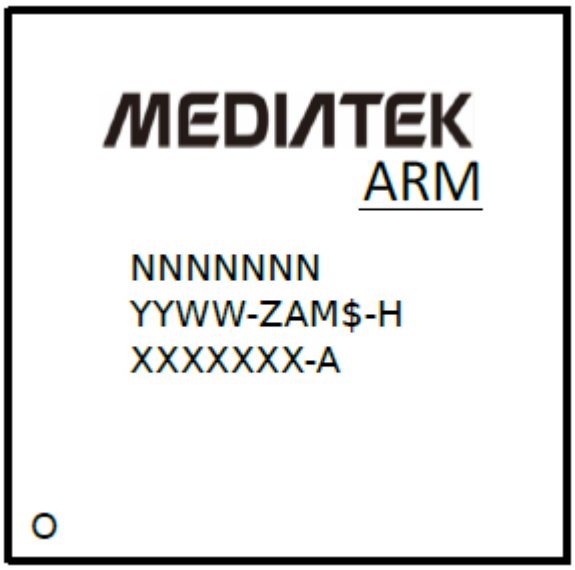


Figure 7-1 Device Top Marking

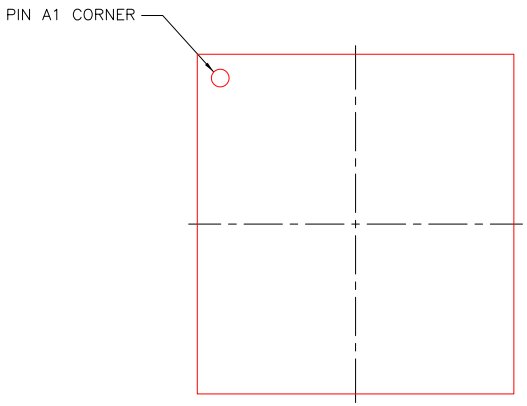
Table 7-2 presents the printed device reference and decoding.

Table 7-2 Printed Device Reference and Decoding

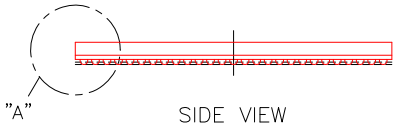
Parameter		Value	Description
NNNNNNN	Part number	MT8385V	Wireless connected multimedia system and IoT platform
YYWW	Date code		2-digits year and week code
ZAM$-H	Internal control code		For internal use only
XXXXXXX-A	Lot number		For internal use only
O	Pin one designator		Pin one location

7.3 Mechanical Drawing

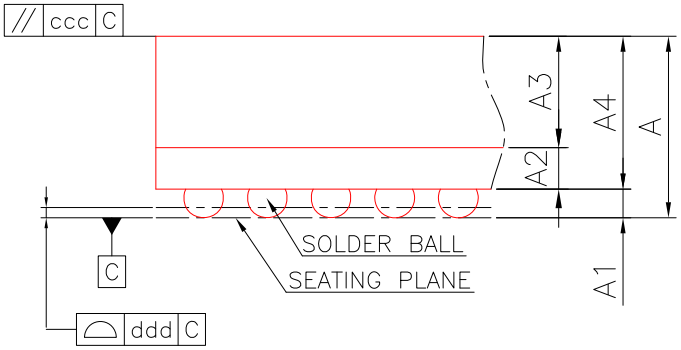
The following figure shows printed device reference diagram (VFBGA 11.0 mm × 11.8 mm, 599-ball, 0.4 mm pitch package).



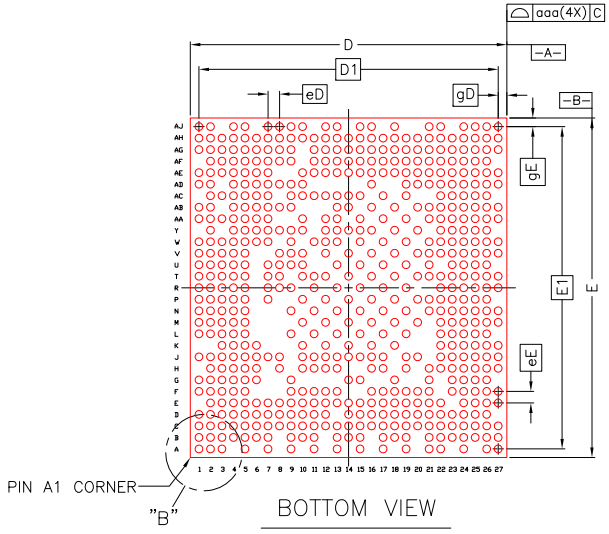
TOP VIEW



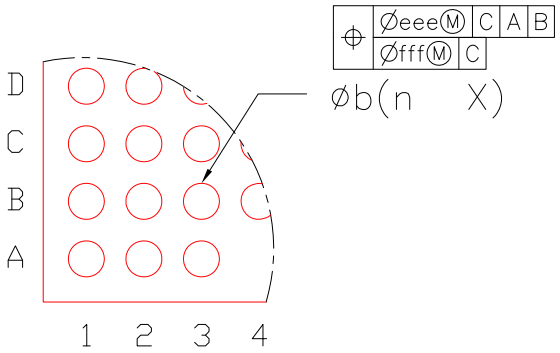
SIDE VIEW



DETAIL : "A"



BOTTOM VIEW



DETAIL : "B"

Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	10.9	11.0	11.1
	Y	E	11.7	11.8	11.9
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.45 Ref.		
Substrate Thickness		A2	0.141 Ref.		
Substrate+Mold Thickness		A4	0.541	0.591	0.641
Total Thickness		A	–	–	0.90
Ball Diameter			0.25		
Ball Stand Off		A1	0.14	0.18	0.22
Ball Width		b	0.22	0.27	0.32
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	599		
Edge Ball Center to Center	X	D1	10.40		
	Y	E1	11.20		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

TITLE	PACKAGE OUTLINE MFC VFBGA 599L 11.0 X 11.8 X 0.9mm		
DWG. NO.	REV.	SHEET	UNIT
MT-SP00630	A	1 OF 2	MM

8 Legal and Support Information

8.1 Related Documents and Products

Documents:

- **MT8385 Audio Design Notice**—Application note for Audio connectivity including system level block diagram, bias and uplink path, schematic and layout recommendations, unused pin handling, and pop noise solutions.
- **MT8385 HW Design Notice**—Application note including schematic examples for peripheral interfaces such as I2C, MSDC, GPIO, UFS, LPDDR3, LPDDR4, Display, Camera, USB, ADC, PWMs, SPI, Audio, and PCB design implementation recommendations.
- **MT8385 PCB Design Guidelines**—Application note including footprint recommendations, PCB stack-up, placement notes, design guidelines for high-speed digital signals and different implementation methods.

Companion chips:

- **MT6358**—Integrated Power Management IC (PMIC)
- **MT6370**—Integrated Power Management IC (PMIC)
- **MT7668**—Highly-integrated, DBDC-enabled 802.11ac MU-MIMO Wi-Fi AP with Bluetooth 5.0, enabling diverse home connectivity
- **MT6631**—Dual-band (2.4 GHz and 5 GHz) 1 x 1 802.11ac Wi-Fi; Bluetooth 5.0, GPS, FM receiver

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